Future Trend in Memory Device

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Where we are?
Everything is Everywhere

Social Service Platform
Mobile
Boundaryless Workplace
Wearable Computer

Nano-Technology + Bio Technology
Natural User Interface : Analog, Gesture, Voice
Smart

Digital Contents Service – Information Overload

N-Screen : Standardized user interface

Convergence and Divergence : Unified function at various user environment

<table>
<thead>
<tr>
<th>Smart Phone</th>
<th>Tablet</th>
<th>Smart TV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Text</td>
<td>Published</td>
<td>Broadcasting &amp; Communication</td>
</tr>
<tr>
<td>Data</td>
<td>Media</td>
<td>Computing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High definition Image</td>
</tr>
</tbody>
</table>
Big Data

Real time unstructured Big Data processing
High capacity network
Visualization

Weather
Geological

Medical Service

3D Map

3D Graphic

3D Game
IT Trends

- Cloud Computing
- Big Data
- Mobile
- Visualization
- Smart
- Natural User Interface
- Convergence & Divergence
- Network
- Digital Contents
Memory requirement
Memory requirement

◆ Cloud Computing & Big Data

→ Memory Centric System
→ High Capacity & Bandwidth Memory
→ SCM (Storage Class Memory)

◆ Visualization

→ Frame Buffer Size & GPU multi-Core
→ Higher Bandwidth/Density Memory

◆ Network

→ Fast Growing Network Traffic
→ High Bandwidth Memory

Source: IDF Beijing (Apr’12)
Memory requirement

◆ Convergence and Divergence

→ Small Form Factor
→ Low Power Consumption

◆ Smart

→ Smart Client and Application Program
→ Higher Bandwidth/Density Memory

◆ Mobile

→ Always on, Anytime on body, Stylish
→ Small Form Factor
→ Low Power Consumption
## Memory Requirement

### Rating of Memory requirements to cope with IT trends

<table>
<thead>
<tr>
<th>IT Trends</th>
<th>High Capacity</th>
<th>High Bandwidth</th>
<th>Low Power</th>
<th>Small Form Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cloud &amp; Big Data</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Middle</td>
</tr>
<tr>
<td>Visualization</td>
<td>High</td>
<td>High</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Network</td>
<td></td>
<td>High</td>
<td>Middle</td>
<td>Middle</td>
</tr>
<tr>
<td>Convergence &amp; Divergence</td>
<td>Middle</td>
<td>High</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Smart</td>
<td>High</td>
<td>High</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mobile</td>
<td></td>
<td></td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>
Memory Barrier
Limited System Power Budget

-> Regulation for Standby power + Operating Power

-> Demands Revolutionary Approach

Energy Star

In 1992 the US Environmental Protection Agency (EPA) introduced ENERGY STAR as a voluntary labeling program designed to identify and promote energy-efficient products to reduce greenhouse gas emissions. Computers and monitors were the first labeled products. Through 1995, EPA expanded the label to additional office equipment products and residential heating and cooling equipment. In 1996, EPA partnered with the US Department of Energy for particular product categories. The ENERGY STAR label is now on major appliances, office equipment, lighting, home electronics, and more.

<table>
<thead>
<tr>
<th>Version 5.0 Energy Efficiency Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Product Type</strong></td>
</tr>
<tr>
<td>Desktops, Integrated Computers</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Source: www.energystar.gov
Performance

Speed up per pin → Wide memory IO

- Computing memory: DDR3 → DDR4
- Graphic memory: GDDR3 → GDDR5
- Mobile memory: LPDDR3

Next?
Capacity

Limits of process technology scaling

→ Stacking Solution
Form-Factor

Scaling & Thin wafer processing

- Smartphone Thickness Trend

2009 2010 2011

- Iphone3G 12.3mm
- Galaxy S 9.9mm
- Iphone4 9.3mm
- Xperia Arc 8.7mm
- Galaxy S II 8.49mm
- 5.4mm

Scaling & Thin wafer processing
Memory Evolution
Memory Evolution

- High Capacity and Bandwidth, Small F/F, Low Power Requirements

- Process technology scaling
  1Xnm? 2xnm?

- Next Generation Transistor
  Multi-gate, FinFET, 3D transistor, Fully depleted SOI, High-K/Metal Gate, Air gap

- 3D chip stack based on TSV
  Speed per pin -> Number of IOs

- Next Generation Memory
  PRAM, MRAM, ReRAM
Next Generation Transfer

**FinFET**

3D tri-gate transistor

---

Fully depleted SOI

Bulk Device

FD-SOI Device

The fully depleted SOI transistor at 20 nm is significantly simpler than even a simplified version of the bulk CMOS transistor.
3D Chip Stack Based on TSV

Packaging Platform

ADVANCED PACKAGING TECHNOLOGIES

Electrical redistribution

3-D integration

Flip-Chip or Wire Bond

WLP

TSV

Wire Bond

Edge traces

Embedded

PoP

Source: Yole Development, *Semicon Korea 2008*
3D Chip Stack Based on TSV

TSV - Through Silicon-Via

Vertical electrical connection passing completely through a silicon wafer or die.

Cases of 3D Memory Stack
3D Chip Stack Based on TSV

Critical Process of 3D Stack Memory

- Bumping
- Temporary Bond & De-bonding
- Thinning & Stacking
3D Chip Stack Based on TSV

Comparison
- 8Gb 5MCP
- 8Gb DDP
- 4Gb SDP

VS.

X4 2Rank 16GB DIMM
8Gb DDP or TSV 5MCP 18ea

X4 2Rank 16GB DIMM
SDP 36ea

Power

Case Temp.

Sl - margin
# 3D Chip Stack Based on TSV

## High Bandwidth

- **Speed per pin**
- **Massive number of IOs**

<table>
<thead>
<tr>
<th>Features</th>
<th>GDDR5</th>
<th>HBM</th>
<th>WIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>2Gb</td>
<td>2Gb</td>
<td>4Gb</td>
</tr>
<tr>
<td>Speed per pin</td>
<td>6Gbps</td>
<td>1Gbps</td>
<td>200Mbps</td>
</tr>
<tr>
<td>Channel</td>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Bank</td>
<td>16</td>
<td>8 / ch</td>
<td>4 / ch</td>
</tr>
<tr>
<td>DQs</td>
<td>32</td>
<td>256</td>
<td>512</td>
</tr>
<tr>
<td># of Stack</td>
<td>1</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>DQs aft Stack</td>
<td>32</td>
<td>1024</td>
<td>512</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>24GB/s</td>
<td>128GB/s</td>
<td>12.8MB/s</td>
</tr>
</tbody>
</table>
## 3D Chip Stack Based on TSV

### Pros and Cons

<table>
<thead>
<tr>
<th>Performance</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Saving</td>
<td>Additional Process</td>
</tr>
<tr>
<td>High Band Width</td>
<td>Low Stacking Yield</td>
</tr>
<tr>
<td>Small Size</td>
<td>Delivery</td>
</tr>
<tr>
<td>High Density</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Form-factor</th>
<th>Micro Joining</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cu Contamination</td>
</tr>
<tr>
<td></td>
<td>Thin Die</td>
</tr>
<tr>
<td></td>
<td>Reliability</td>
</tr>
</tbody>
</table>
Test Challenges

- Multi-wafer burn-in for reliability and yield
- Testing of VIA defects at wafer level
- Probing on the u-bump for mission mode test
- KGSD test (Wafer or Package)
- Memory BIST, BIRA, BISR for memory test in SiP
Next Generation Memory

Requirements for Next Generation Memory

- Maintain same memory budget in a system
  Cost of new material, Scalable for Generations

- Meet performance trends

- Backward compatible interface
  DDR4 like?

- More Moore and/or More than Moore
  Geometrical Scaling / Extends the benefits of Moore’s Law

- Green Product
  Healthy, Safe, Environment-friendly
## Next Generation Memory

### Promising Candidates

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PCRAM</strong></td>
<td>- Non-Volatile</td>
</tr>
<tr>
<td>(Phase-Change RAM)</td>
<td>- Medium Performance</td>
</tr>
<tr>
<td></td>
<td>- Storage Class Memory</td>
</tr>
<tr>
<td><strong>STT-MRAM</strong></td>
<td>- Non-Volatile</td>
</tr>
<tr>
<td>(Spin Transfer Torque RAM)</td>
<td>- DRAM and NAND alternatives</td>
</tr>
<tr>
<td></td>
<td>- Expensive</td>
</tr>
<tr>
<td><strong>ReRAM</strong></td>
<td>- Non-Volatile</td>
</tr>
<tr>
<td>(Resistive RAM)</td>
<td>- NAND alternatives</td>
</tr>
<tr>
<td></td>
<td>- High Density</td>
</tr>
</tbody>
</table>
Next Generation Memory

**PCRAM**

Phase-Change Material
- More than 2 phases with different properties
- Repeatedly switchable between phases

Amorphous phase
- High electrical resistivity
- Low optical reflectivity

Crystalline phase
- Low electrical resistivity
- High optical reflectivity

In 1960s, Phase-Change material was demonstrated.
In 1990s, discovering of fast crystallization materials draws industrial attention.
Next Generation Memory

PCRAM

I-V Curve of Phase-Change Material

① Applied voltage is below Vth,  
   -> Low conductivity amorphous state

② Applied voltage is over Vth,  
   -> High conductivity state

③ Lower the voltage,  
   -> Return to the low conductivity amorphous state

*. Threshold switching is the key property of phase-change material  
   : Impact ionization + Carrier recombination
Next Generation Memory

PCRAM

Cell Structure

1) Contact minimized cell: Minimize the size of electrical contact
   Low heat loss (heat concentrates on the small contact spot)

2) Volume minimized cell: Minimize the size of Phase-Change material
   Low RESET current, High Endurance
**Next Generation Memory**

**PCRAM**

**Cell Operation**
- **RESET**: Amorphous highly resistive state
  - High power pulse current
  - Temp. > T-melting
- **SET**: Crystalline highly conductive state
  - Moderate power and long duration pulse current
  - T-crystallization < Temp. < T-melting
- **READ**: Sensing the resistance difference between the two state
  - Very low power current

![Diagram of PCRAM cell operation](image)

- **Bit Line**
- **Word Line**
- **Access Device**
- **Phase-Change Material**
- **Crystallization**
Next Generation Memory

PCRAM

Critical parameters for PCRAM

- Reset Current
- SET and RESET resistance distribution & Ratio
- Endurance (RESET/SET switching cycles)
- SET speed: Write Speed
- Data Retention time (Retain the amorphous state)

Diagram:

- Bit Line
- Word Line
- Access Device
- Phase Change Material
- Crystallization

32/44
Next Generation Memory

STT-MRAM

Spin Transfer Torque
- Each electron has spin.
- Electrons flowing in ferromagnetic components are polarized.
- Spin-polarized current modifies the orientation of a magnetic layer.

Magnetic Tunnel Junction
- Ferromagnet – Insulator layer – Ferromagnet
- If insulator layer is thin, electrons tunnel from one ferromagnet into the other

The orientation of the magnetization affects the amount of current flow.
Next Generation Memory

STT-MRAM

Cell Structure

- MTJ (Magnetic Tunnel Junction)
- Thick Ferromagnetic Layer (Fixed Layer)
- Thin Ferromagnetic Layer (Free Layer)
- Thin Insulator Layer (Tunnel Barrier)
Next Generation Memory

**STT-MRAM**

**Cell Operation**
- Conventional MRAM
  - Magnetic field generated by Write Word Line
- STT-MRAM
  - Spin transfer effect by spin-polarized current flowing through MTJ

![Diagram of MRAM and STT-MRAM cells](image-url)
Next Generation Memory

STT-MRAM

Critical parameters for STT-MRAM

- TMR (Tunnel Magnetoresistance)
  Read margin & speed
- Write current density
  Write current scales down with cell size
- \( V_{bd} \): MTJ breakdown voltage
  Life time, endurance
- Thermal stability
  Data retention
Next Generation Memory

ReRAM

Negative differential resistance (NDR)
- Increased voltage/current result in radical decrease of current/voltage

CCNR (Current Control NDR)
VCNR (Voltage Control NDR)

Switching Mechanism
- Conducting Filament model
  Metallic filament
- Electronic Switching model
  Charge trap / de-trap etc.
Next Generation Memory

ReRAM

I-V curve of ReRAM at DC sweep mode
- Switch between low resistance state and high resistance state as the applied voltage sweeps.
- $V_{\text{read}}$: Low resistance state (a)
- $V_{\text{reset}}$: High resistance state (c)
- $V_{\text{set}}$: Low resistance state (d)
Next Generation Memory

ReRAM

Cell Structure
- Resistive Element
  MIM (Metal / Insulator / Metal)
- Cross Point cell
- 1 Diode 1 Resistor
- 1 TR 1 Resistor
Next Generation Memory

ReRAM

Cell Operation
- **RESET**
  - High voltage from Word line to Bit line
  - High resistive state
- **SET**
  - High voltage from Bit line to Word line
  - Low resistive state
- **READ**
  - Low voltage from Bit line to Word line
  - Non-destructive operation

![Diagram of ReRAM cell operation](image)
Next Generation Memory

ReRAM

Critical Parameters for ReRAM

- Forming Voltage
- SET and RESET resistance distribution & Ratio
- Endurance (RESET/SET switching cycles)
- Sneak Current
Next Generation Memory

Test challenges of NGM

• DDR4-like or DDR4 interface eases ATE options

But
• Inexperienced Material and Geometry behavior
• Unknown Yield and Reliability model
• Timely Test Baseline and Quality Control

are challenging issues.

In-depth fault modeling and studies for the behaviors of faults are required.
Summary

- Traditional Memory Trends are low power, high bandwidth, high density, small form factor
- 3D memory technology based on TSV is emerging
- Requirements for Next Generation Memory are
  - Maintain same memory budget in a system
    - Cost of new material, Scalable for Generations
  - Meet performance trends
  - Backward compatible interface
    - DDR4 like?
  - More Moore and/or More than Moore
    - Geometrical Scaling / Extends the benefits of Moore’s Law
  - Green Product
    - Healthy, Safe, Environment-Friendly
Thanks