Digital IO PAD Overview and Calibration Scheme

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Contents

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2. IO Structure
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4. Conclusion
• IO circuits
  • In each pad, several i/o circuits are implemented.
  • In implementation, digital signals are connected in the inner side of pad.
IO circuits
• PADs require many kinds of power and signal rings.
  • Ex) calibration signals required to control unit driving strength.
  • Special PAD is required to generate control signals.

[Diagram showing IO circuits with layers for calibration n1, calibration n2, calibration n3, VREF, VDD, VSS, bonding area, VDDQ, VSSQ]
Introduction—IO Structure

- Circuits in I/O pad
  - ESD (Electrostatic discharge) diode
  - ESD (Electrostatic discharge) resister
  - Output driver
  - Input receiver
  - Level shifters for digital signals
Introduction—ZQ Calibration

• Requirement for high speed IO circuits
  • Impedance matching should be kept.
  • PVT (Process, Voltage, Temperature) variation can be critical.

• Reliable output driver
  • Driving strength should be maintained regardless of PVT variation.
  • Especially, voltage and temperature variations are more critical.
    • Good process can guarantee reasonable variation.
  • For mobile application, on-diet termination should be avoided due to high power consumption.
    • ZQ calibration is more valuable.
ZQ calibration

- Practically, standards of DDR3 and DDR4 DRAM should support ZQ calibration.
- Compared to ZQ resistor (RZQ = 240 Ohm), the strength of unit driver is calibrated.
- By dividing the impedance of unit driver, Ron is also calibrated.

Variation should be reduced!!
IO Structure
IO Structure

• IO modes:
  • Slew rate control
  • Driving strength for p and n drivers
  • Unit driver strength calibration for p and n drivers
  • Receiver reference voltage
  • Schmitt trigger
  • On die termination
  • Functions for turning on/off drivers/receivers
IO Structure

• Slew rate control
  • Slew rate: maximum voltage change per unit time.
  • Strong pre-driver charges or discharges the gate of driver fast.
    • Large slew rate → Large eye
  • However, the problem of overshoot and undershoot can happen.
IO Structure

• Slew rate control
  • A pad has driver and pre-driver.

• Slew rate control is related to pre-driver.

![Diagram](image)

- strong pre-driver
- weak pre-driver
- driver
- PAD
IO Structure

- Slew rate control
  - What is the good slew rate control?
    - The overshoot and undershoot specification should be met.
    - Large slew rate increases eye, but harms power integrity.
  - Considering various cases, different slew rate control modes are implemented in drivers.
    - Ex) #pads for a driver can be different according to implementation.
    - Different capacitance and inductance can be given.
**IO Structure**

- Driving strength for p and n drivers
  - Like slew rate, driving strength can be another factor for affecting overshoot and undershoot.
  - Depending on the capacitance of pads, driving strength can be adjusted.

![IO Structure Diagram]

- From pre-driver to PAD
  - p-driver
  - n-driver
- VDD
- VCC
IO Structure

• Driving strength for p and n drivers
  • Multiple unit drivers are adopted for controlling driving strength.

• Due to area cost, #options is limited.
  
  strength control
  
  → Unit-driver x n
  → Unit-driver x 1
  → Unit-driver x 2
  → Unit-driver x 4
IO Structure

• Unit driver strength calibration for p and n drivers
  • Each unit driver can have small p–drivers and n–drivers to calibrate unit driver strength.
IO Structure

• Unit driver strength calibration for p and n drivers
  • Duty ratio is related to the unit driver strength calibration.

• Unit driver with strength calibration should have separate pre-driving inverters for p-driver and n-driver.

• All pads can share the same unit driver strength calibration codes.
  • Using metal rings, the signal can be supplied to each unit drivers.
**IO Structure**

- Receiver reference voltage
  - For differential I/O, voltage reference is not required.
  - However, two pads are required.
    - Critical for pad limit IC implementation!!

- Pseudo differential IO (ex. SSTL) can be common.
  - SSTL: Stub Series Terminated Logic

*Figure 2: Alternative Termination for SSTL*
IO Structure

- Receiver reference voltage
  - A comparator is adopted for pseudo differential receiver.
  - Reference voltage is generated in the host side.
  - Voltage divider is common solution.

Figure 2: Alternative Termination for SSTL
IO Structure

- Receiver reference voltage
  - Sometimes, internal reference voltage generator should be adopted.

- The integrity of the generated reference voltage is key.
  - Special care is required in IC implementation.

- Reference voltage level can be calibrated for fining maximum eye.
  - For compensating receiver input high/low voltage level.
  - Controlled reference voltage levels are required!!
**IO Structure**

- **Schmitt Trigger**
  - Schmitt trigger suppresses input noise with threshold voltage.
  - However, receiver input delay can increase with Schmitt trigger.
IO Structure

• Schmitt Trigger
  • Nowadays, basic idea of SSTL IO does not adopt Schmitt trigger on/off option.
  
  • For CMOS receiver, Schmitt trigger is common. However, CMOS receiver has large input delay, compared to differential receiver.

  • However, small hysteresis is required in the receiver of SSTL IO.
IO Structure

• **On Die Termination**
  - For signal integrity, on die termination (ODT) is common for external RAM.
    - For internal RAM, ODT is avoided due to high power consumption.
  - Resistors are implemented for the impedance matching.
IO Structure

• On Die Termination
  • The serial resistors consumes large currents in receiver sides.
  • For minimizing IO energy consumption, ODT should be avoided.
    • Instead, other skills for enhancing signal integrity are required.

출처: www.rambus.com
IO Structure

- Functions for turning on/off drivers/receivers
  - Current consumption can be proportional to the number of pads.
  - For differential receiver, comparator should be turned off for idle or power saving mode.
  - Slow CMOS receiver is adopted for power saving mode.
IO Structure

• Functions for turning on/off drivers/receivers
  • Leakage current in PAD can be possible.
  • To enhance yield in field of energy limitation, unused drivers can be turned off for reducing leakage current through pads.
ZQ Calibration Scheme
• Driving strength of IO drivers (Ref: Miron TN–41–02)

Parallel unit drivers

Parallel unit drivers

Unit Driver
Turn on/off for scaling impedance
ZQ Calibration Scheme

• For supporting ZQ calibration in IO drivers
  • 240 ohm homogeneous unit drivers should be programmable.
  • By parallelizing unit drivers, target impedance can be obtained.

• For supporting ZQ calibration in device (ex, DDR3)
  • ZQ calibration commands are equipped.
  • Ex) Micron DDR3

Table 1: ZQ Command Truth Table

<table>
<thead>
<tr>
<th>Function</th>
<th>Abbreviation</th>
<th>CKE</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Previous Cycle</td>
<td>Next Cycle</td>
<td>CS#</td>
<td>CAS#</td>
<td>RAS#</td>
<td>WE#</td>
<td>BA0-BA3</td>
<td>A13-A15</td>
<td>A12</td>
<td>A10</td>
</tr>
<tr>
<td>ZQ CALIBRATION LONG</td>
<td>ZQCL</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>ZQ CALIBRATION SHORT</td>
<td>ZQCS</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
</tr>
</tbody>
</table>
ZQ Calibration Scheme

- **ZQ calibration command**
  - **ZQ calibration long**
    - Used for full calibration at initial system power up when device is in a reset condition.

- **ZQ calibration short**
  - Tracks the continuous voltage and temperature change.

- **Data bus when ZQ calibration command is issued**
  - Memory data bus remains completely idle and quiet.
    - To suppress the noise for calculating ZQ calibration
  - Long idle time
    - 256 cycles for ZQCL
    - 64 cycles for ZQCS
ZQ Calibration Scheme

- ZQ calibration timing

Idle memory data bus
ZQ Calibration Scheme

ZQ calibration controller

- Obtained code
- Programmable code
- Comparator
  - Vref_p
  - Vref_n

p-unit driver

External Resistor (240ohm)

n-unit driver
ZQ Calibration Scheme

- **External resistor**
  - 240 ohm external resistor for calibrating unit driver
  - Used for obtaining code for p-unit driver

- **ZQ calibration controller**
  - Full digital block for controlling unit drivers
  - According to programmable transistors in a unit driver, the width of calibration code is determined.
  - Digital noise can be harmful for comparator
    - Suitable noise blocking is required.
ZQ Calibration Scheme

- **Steps for obtaining code**
  - **Step 1**
    - Decrease impedance of p-unit driver using programmable code
    - When output of comparator is changed to high, the programmable code is determined for p-unit driver.
  - **Step 2**
    - Apply the p-unit driver code
    - Increasing impedance of n-unit driver using programmable code
    - When output of comparator is changed to high, the programmable code is determined for n-unit driver.
  - **Step 3**
    - The obtained code is outputted for IO drivers.
Example of obtaining code

Below example, code = 4 is the first value of high.

By increasing code step by step, code = 4 can be the first value.

<table>
<thead>
<tr>
<th>Comparator output</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>code = 7</td>
</tr>
<tr>
<td>High</td>
<td>code = 6</td>
</tr>
<tr>
<td>High</td>
<td>code = 5</td>
</tr>
<tr>
<td>High</td>
<td>code = 4</td>
</tr>
<tr>
<td>Low</td>
<td>code = 3</td>
</tr>
<tr>
<td>Low</td>
<td>code = 2</td>
</tr>
<tr>
<td>Low</td>
<td>code = 1</td>
</tr>
<tr>
<td>Low</td>
<td>code = 0</td>
</tr>
</tbody>
</table>

code: 0 → 1 → 2 → 3 → 4 (obtained code: 4)
ZQ Calibration Scheme

- Short calibration time
  - Instead of changing impedance step by step, binary code can be adopted.
  - Binary code can be generated from ZQ calibration controller.
  - After Starting from center value, then, finishing for first value of high.

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</tr>
<tr>
<td>High</td>
<td>code = 4</td>
</tr>
<tr>
<td>Low</td>
<td>code = 3</td>
</tr>
<tr>
<td>Low</td>
<td>code = 2</td>
</tr>
<tr>
<td>Low</td>
<td>code = 1</td>
</tr>
<tr>
<td>Low</td>
<td>code = 0</td>
</tr>
</tbody>
</table>

code: 4 \rightarrow 3 \text{(obtained code: 4)}
ZQ Calibration Scheme

• Need for short calibration time
  • Unlike process and temperature variation, voltage drift can happen in a short time.

• Another way to suppress voltage drift
  • Large on-chip capacitor (100pF~) can be effective.
    • Due to the small impedance of unit driver (about 240 ohm), on-chip capacitor should be limited.
  • Off-chip capacitor
    • Small MLCC can be attached close to the power source.
    • Sometime, due to the size limitation (ex Flash memory card), off-chip capacitor can be impossible.
ZQ Calibration Scheme

- **Cause of error (ex. < 10 % DDR3 RAM)**
  - ZQ external resistor: 1%
  - Difference between programmable codes
    - Ex) 250 ohm for code = 4, 230 ohm for code = 5 → 20 ohm difference in unit driver. In this case, 8.3% error can be caused.

- **Impedance in path towards ball**
  - Impedance exists in path towards ball
  - Due to the variation of path length, error can happen.
  - In MCP (multi-chip package), paths between PAD and ball can be different.
• **Minimization of Error**
  - ZQ external resistor: cannot be avoided (according to spec)

• Impedance in path towards ball
  - Impedance in the path should be estimated in advance.
  - The estimated impedance in the path should be considered for obtaining calibration code.
ZQ Calibration Scheme

• Minimization of Error
  • Difference between programmable codes
    • The size of calibration code and programmability of unit driver can be increased.
      • 3-bit unit driver → 8 different values
      • 10-bit unit driver → 1,000 different values
  • When increasing programmability, hardware overhead in IO circuit also increases.
    • Suitable size and programmability should be considered.
  • Regularity in programmable code is also important!
    • IO design should consider the regularity of programmable values.
    • Ex) 250 ohm for code = 4, 230 ohm for code = 5 → 20 ohm difference in unit driver.
    • Ex) 290 ohm for code = 2, 260 ohm for code = 3 → 30 ohm difference in unit driver.
ZQ Calibration Scheme

• Test of ZQ calibration block
  • Test mode for ZQ calibration should be provided.

  • External analog test point can be adopted.
    • Ball for external ZQ resistor can be a good test point.

• Considering PVT variation, characteristics of IO driver should be proved.
  • Before mass production, characteristics of IO driver should be proved with large samples. (1,000EA~)
  • Unlike old DC test, test of ZQ calibration block can be performed with various environments.
ZQ Calibration Scheme

• EDS vs. Package
  • Impedance in path towards ball and ZQ resistor should be considered.
  • In EDS, the characteristics mentioned before cannot be considered.
  • In real, the evaluation of signal integrity can be performed in board level.
    • Driving strength from ZQ calibration should be considered.
Conclusion

• Why is the understanding of IO structure important?
  • A lot of circuits are contained in IO pads.

• What is ZQ calibration?
  • IO driving strength is maintained regardless of PVT variation.

• Practical design in ZQ calibration
  • For short calibration time, binary search can be adopted.
  • Voltage drift can be more critical than process and temperature variations.
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