TSV:PKG (Device) 변화에 따른
Test issue

11'th Nov, 2009

CONFIDENTIAL

All Rights Reserved - Advantest Corporation

REV2.0

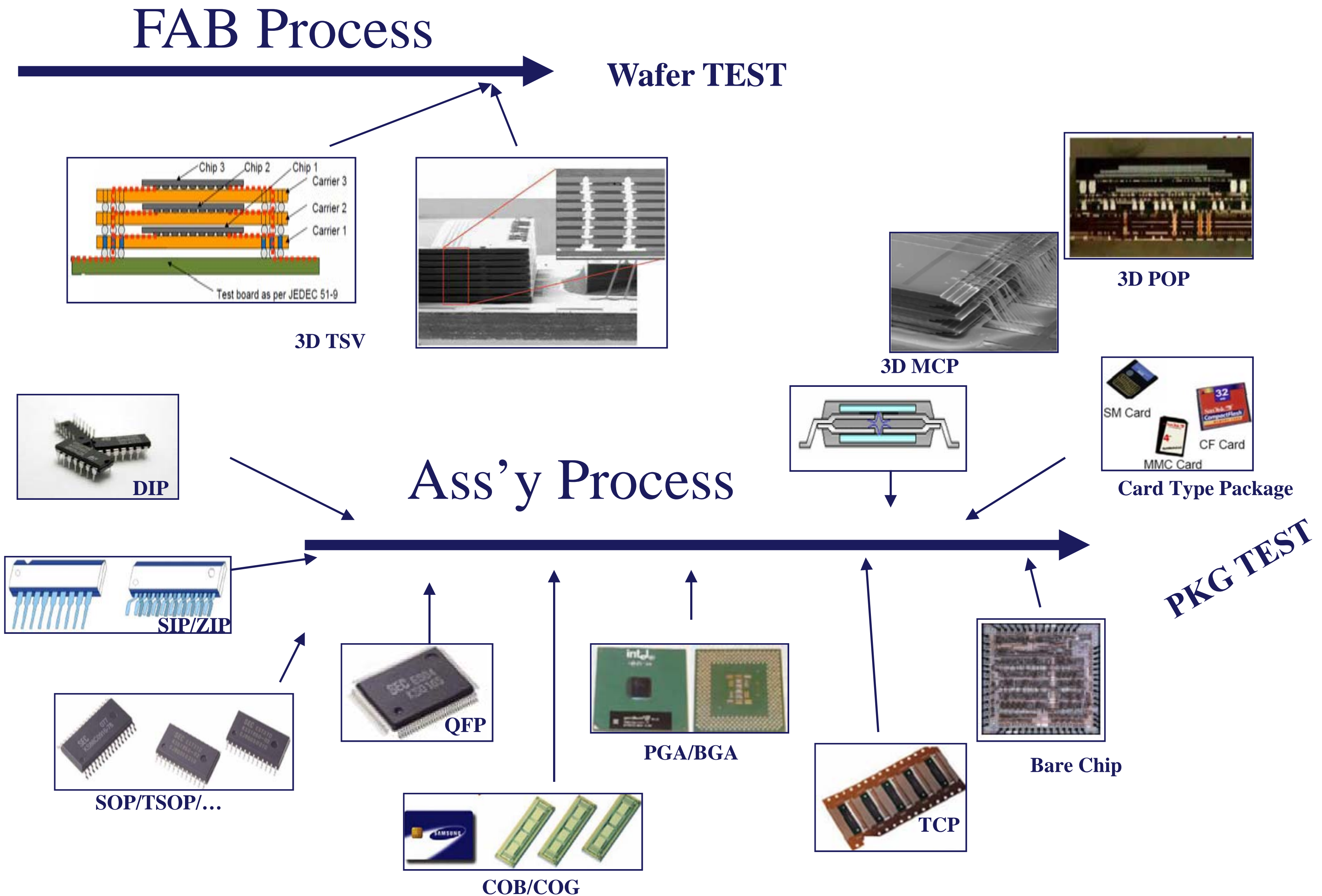
Various Applications

Rights Reserved - Advantest Corporation

CONFIDENTIAL

PKG TREND

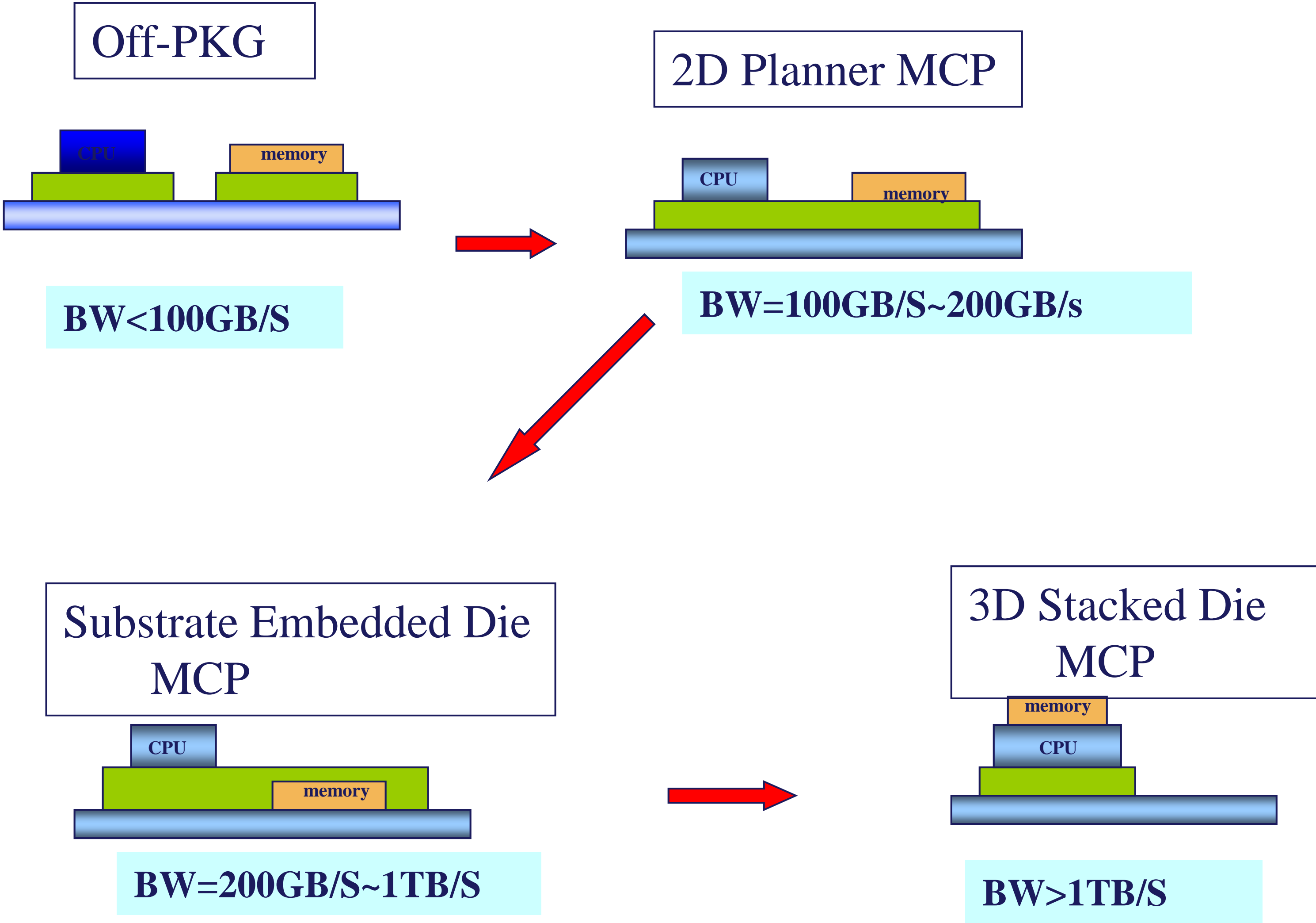
ADVANTEST



All Rights Reserved - Advantest Corporation

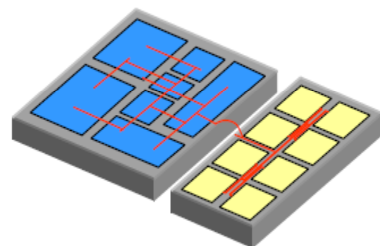
REV2.0

CONFIDENTIAL

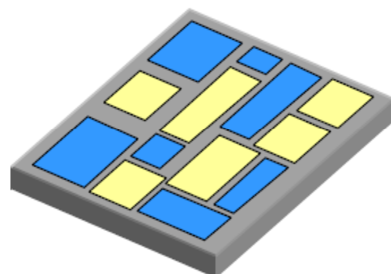


All Rights Reserved - Advantest Corporation

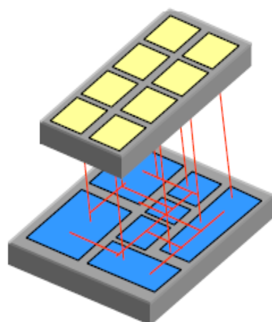
CONFIDENTIAL



2D interconnect:
- Large form factor
- Long lines/ shared bus



SOC solution:
- Reduced system size
- Increased performance
- Increased device cost



3D stack:

3D Stack

■ Wafer Stack

-.Base on Wafer Fabrication & Wafer Bonding.

-.Minimize interconnection length.

-.Ultra fine-pitch interconnection.

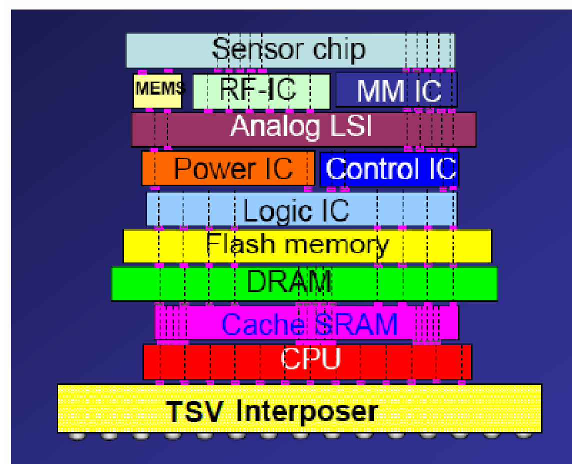
->Yield: depend on each wafer yield

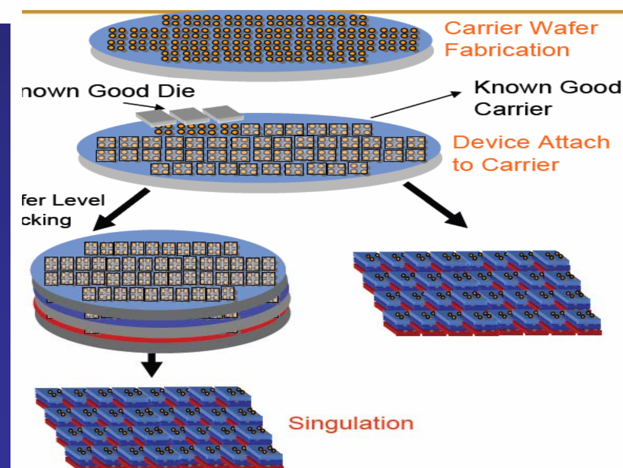
->Each wafer & Chip must be same size

■ **Chip Stack**

-.Heterogeneous integration different wafer size& Die size

different substrate (Si vs GaAs)





(Source: Zycube)

All Rights Reserved - Advantest Corporation

CONFIDENTIAL

TEST Mission

ADVANTEST

1.Design Evaluation

(Engineering Trial & setup)

- **Design** — Probe Card / Test Flow / Program

- **Evaluation**
- **Test Condition**

- **Failure analysis (Speed/Address/Current)**

2.Mass Production Set-Up

- **Correlation**
- **Capacity**
- **Specification Document**
- **Start-up**

3.Efficiency & Improvement

1. Tool Design and Development support

- Design for Probe Card and optimization
- Proposal for cost effective card / board etc

2. Program Development

- Proposal for optimum redundancy routine (memory)
- Development for Wafer Test and final test
- Program conversion

3. Evaluation and Analysis

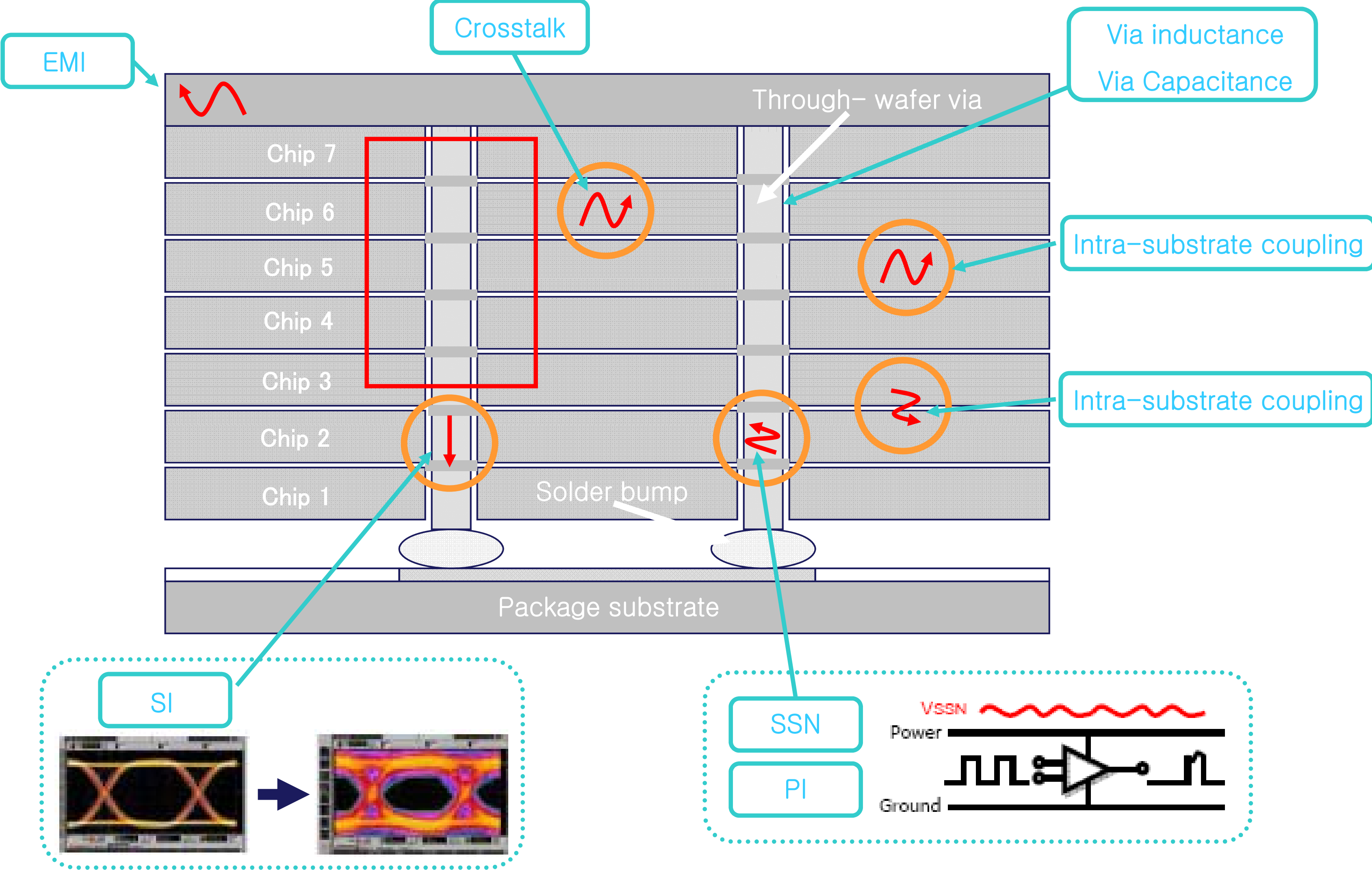
- Collection for evaluation data and report service
- Collection for Fmap/ bin data and report service

All Rights Reserved - Advantest Corporation

CONFIDENTIAL

Design Evaluation

ADVANTEST



All Rights Reserved - Advantest Corporation
REV2.0
CONFIDENTIAL

Design Evaluation

ADVANTEST

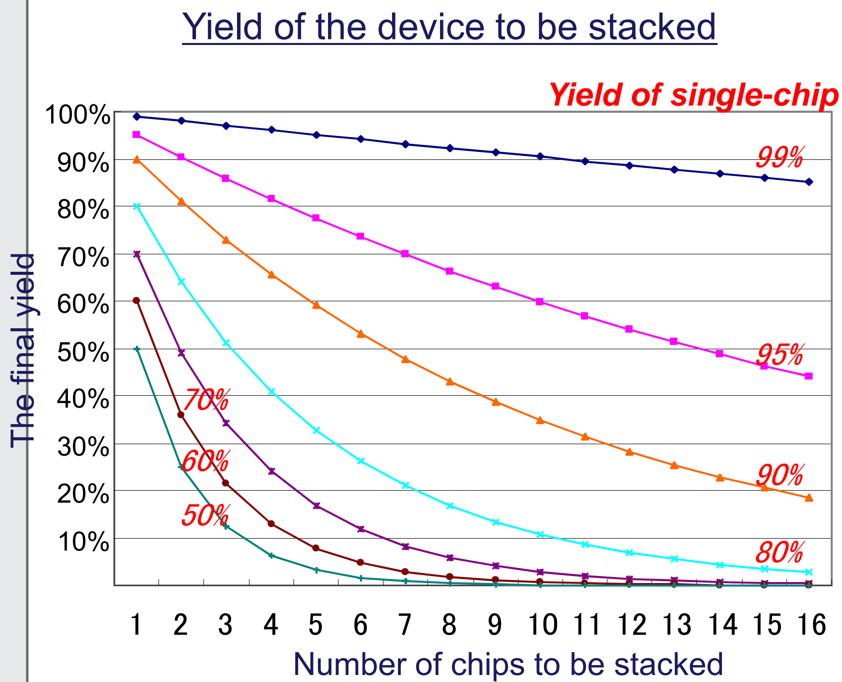
	Geometrical	Mechanical	Thermal	Electrical
IC		Low-K damage	Limited area for heat removal	High currents supplied
IC to interposer	Peripheral I/O pitch: to 20 nm Are-array pitch: to 50 nm	Optimal underfill material and spring-like interconnects for thermal expansion compatibility(3ppm/℃)	Heat conduction through underfill/flip-chip	Scaled flip-chip solder connections pose electromigration (EM) risk
Interposer	Compatible w/chip I/O:20-40 μm wiring density	Scaled micro-BGA for thermal expansion compatibility w/PCB	Improved thermal conductivity based on material	Low inductance, low resistance; capacitive decoupling required
Interposer to PCB	PCB Compatible Pitch:>500		Heat spread through solder joints	Large number power/ground solder balls required to limit EM
PCB		17ppm/℃	Through PCB is main heat path for low-/medium-power devices	

All Rights Reserved - Advantest Corporation REV2.0 CONFIDENTIAL

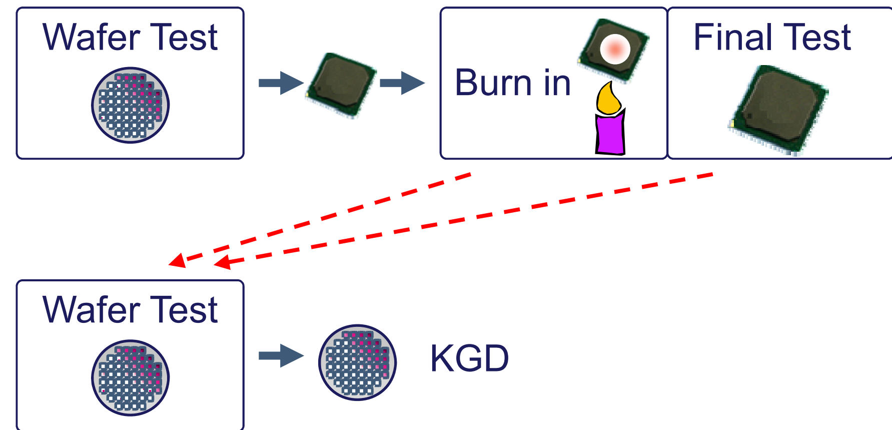
Mass Production set-up

ADVANTEST

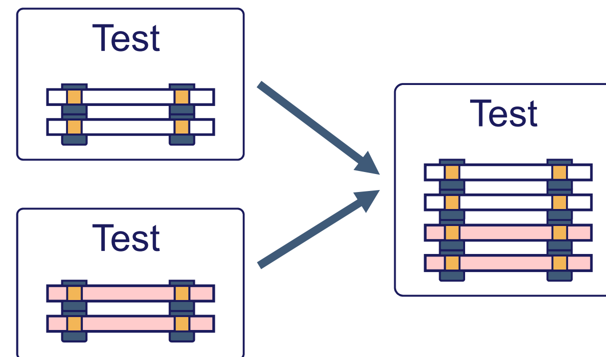
KGD is necessary



1. Total Test at once ?



2. Test during the stacking process ?

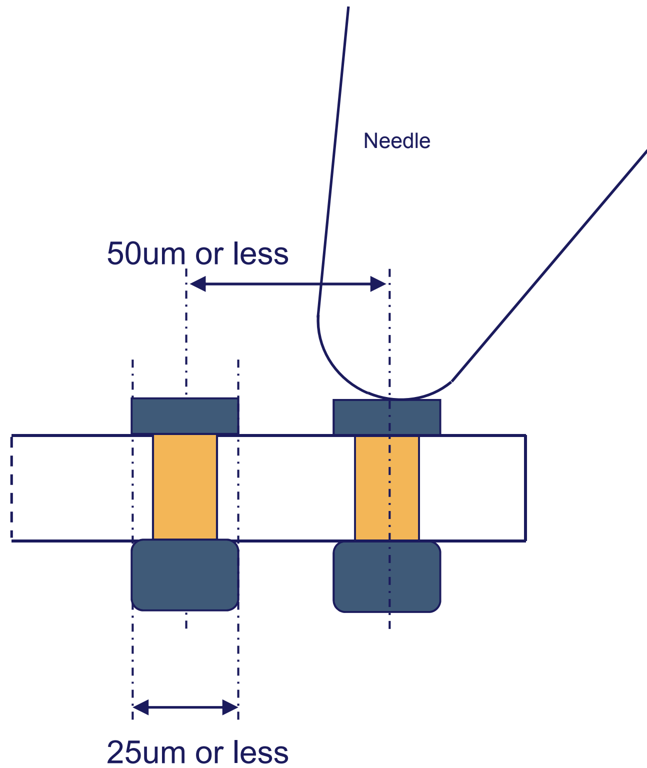


All Rights Reserved - Advantest Corporation
REV2.0
CONFIDENTIAL

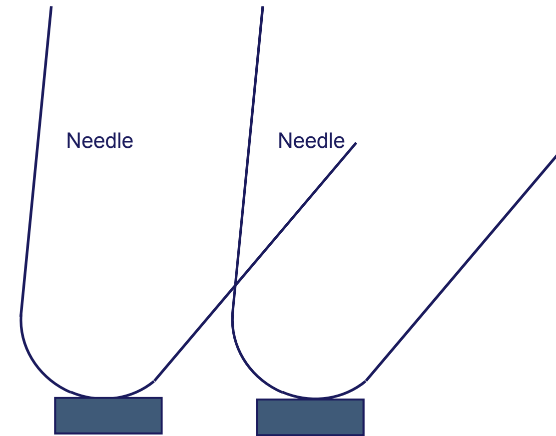
Mass Production set-up

ADVANTEST

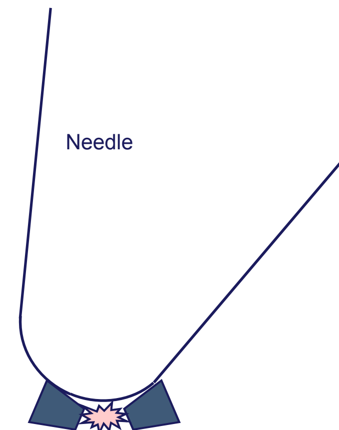
Narrow contact pitch and small bumps



1. Still use needle ?



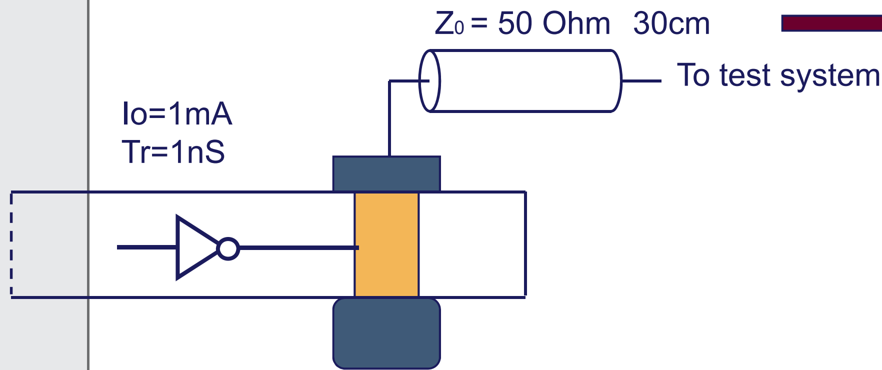
2. ultra-low pressure ?

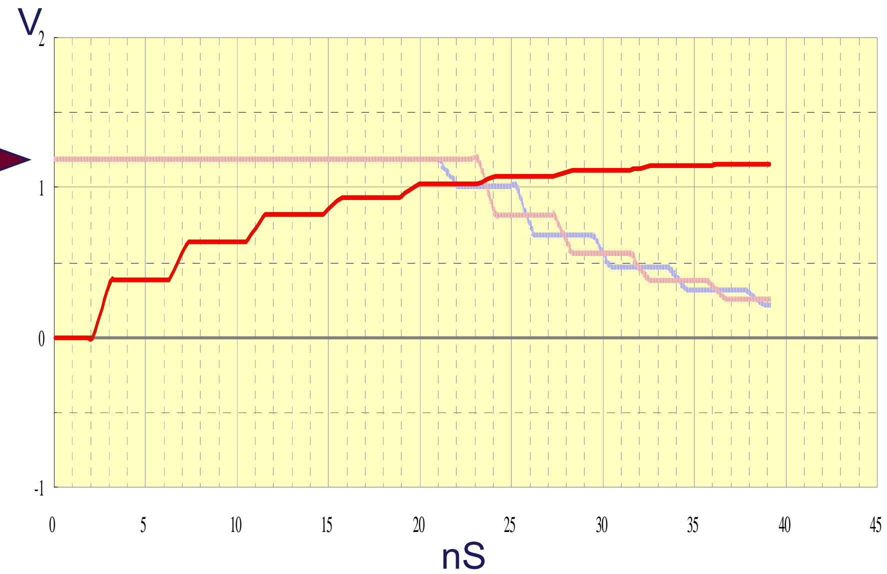


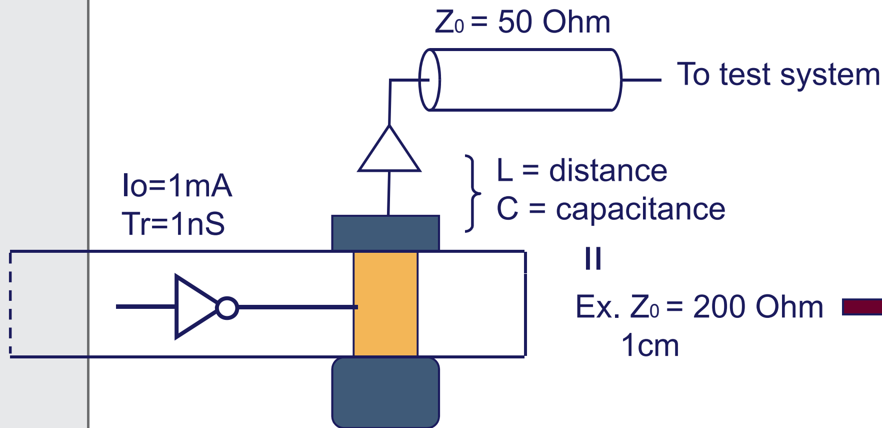
All Rights Reserved - Advantest Corporation
REV2.0
CONFIDENTIAL

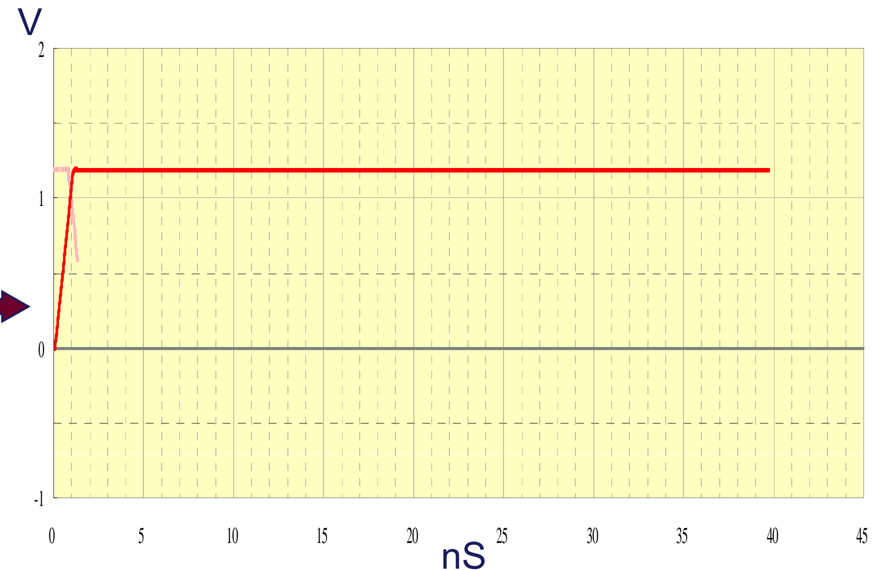
Mass Production set-up

Limit the drive capacity







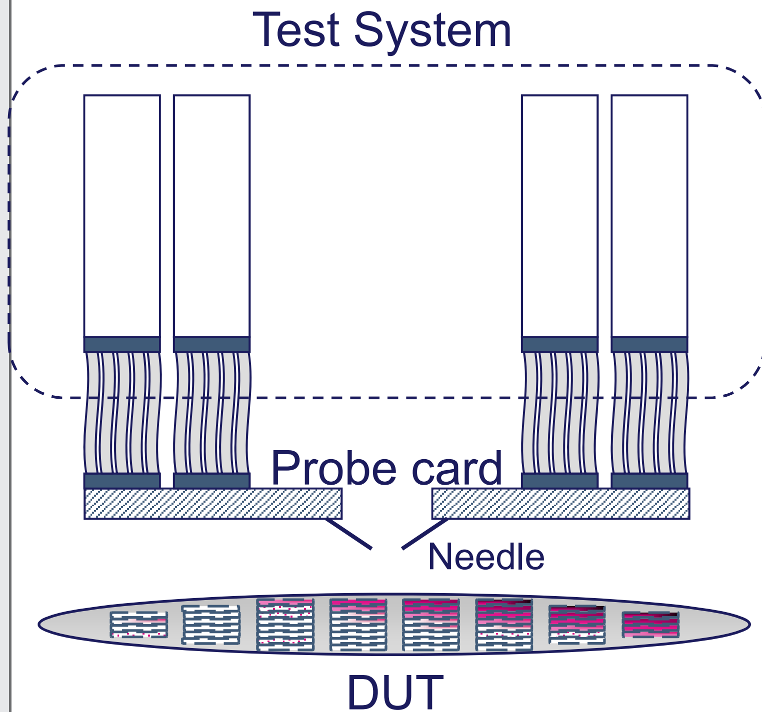


All Rights Reserved - Advantest Corporation
REV2.0
CONFIDENTIAL

Mass Production set-up

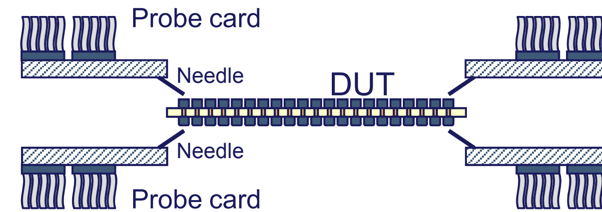
ADVANTEST

increasing the number of signal



1. Over 2000 signals/chip ?

   how many pins?
   both side contact ?

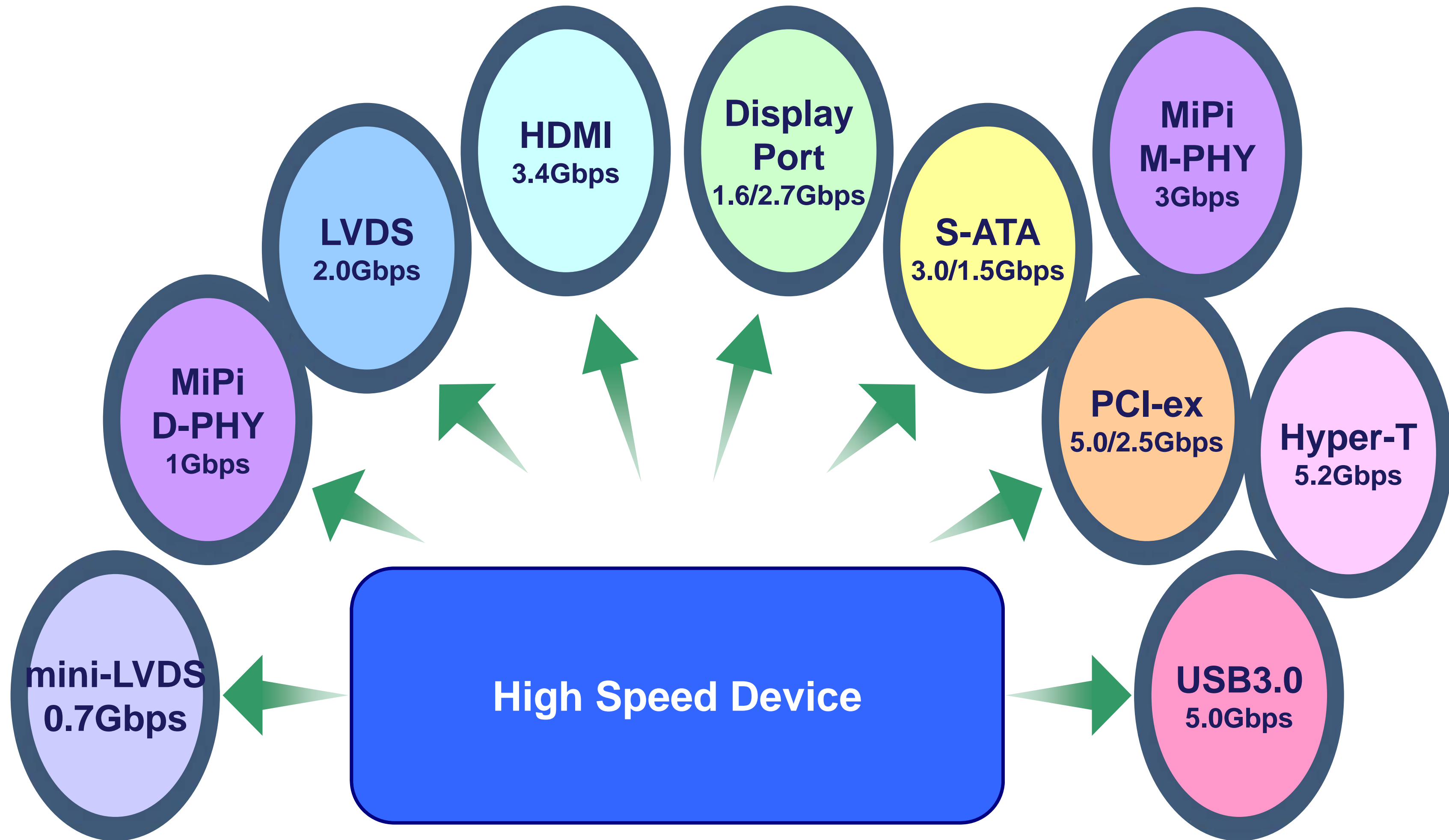


2. Parallel test for cost reduction ?

   ex. 2000signal X 64 chip
   =128000 contact

All Rights Reserved - Advantest Corporation REV2.0 CONFIDENTIAL

Summary



All Rights Reserved - Advantest Corporation

CONFIDENTIAL

Thank You Very Much

All Rights Reserved - Advantest Corporation

CONFIDENTIAL