



# Test Cost Reduction

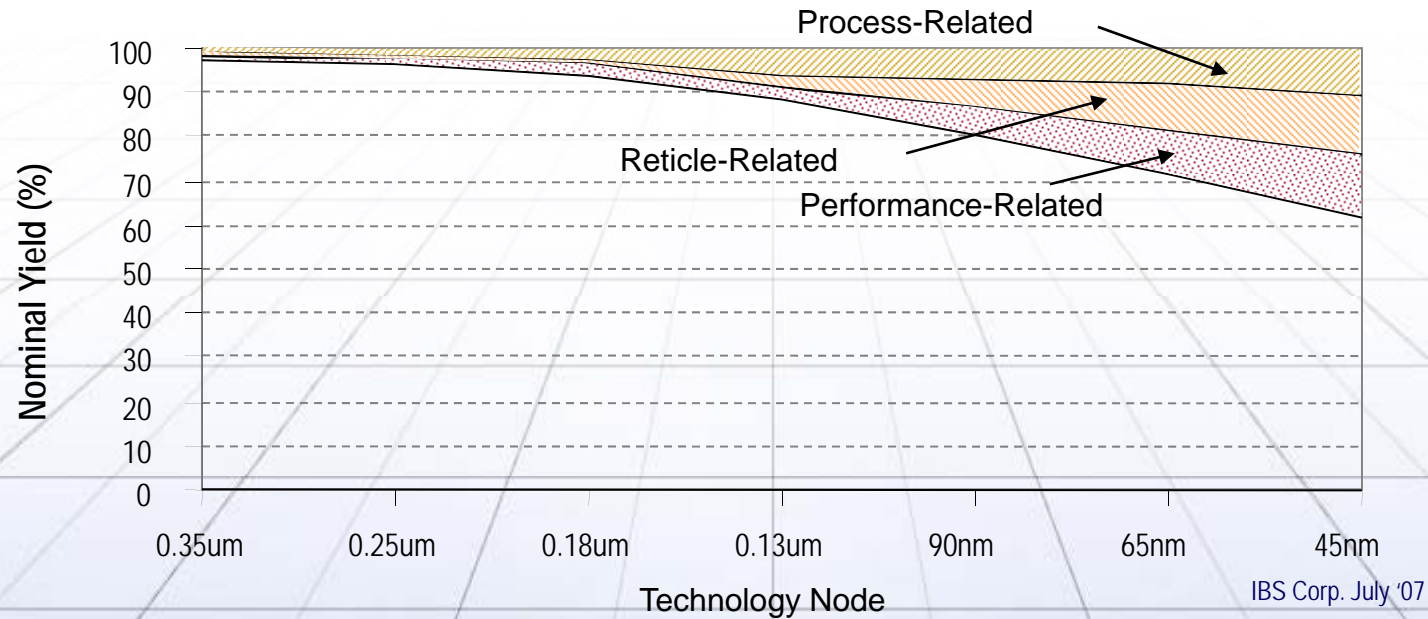
**LG Electronics**  
**Lee, Yong**

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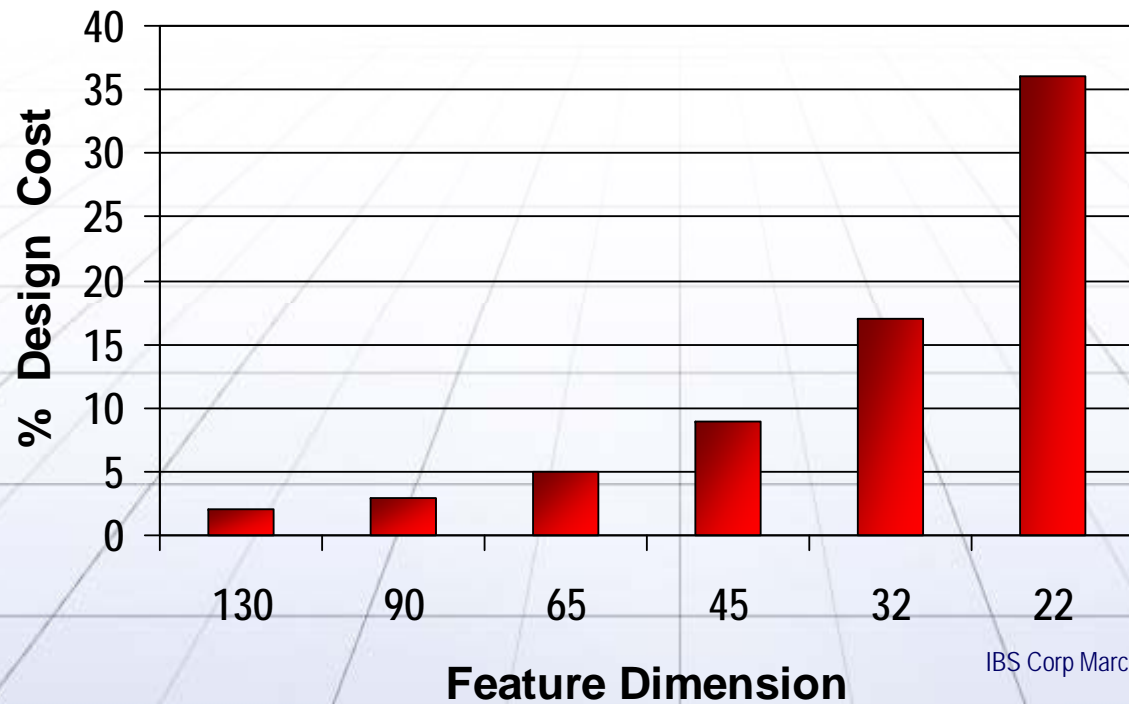
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  - Low cost ATE
  - Test time
  - Reuse a large block
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  - Power-Aware DFT
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- **Future works**

# Introduction



- **Un-modeled signal integrity faults**
  - Need for accurate at-speed test
  - High Cost ATE
  - Huge test patterns are required for un-modeled faults

# Introduction

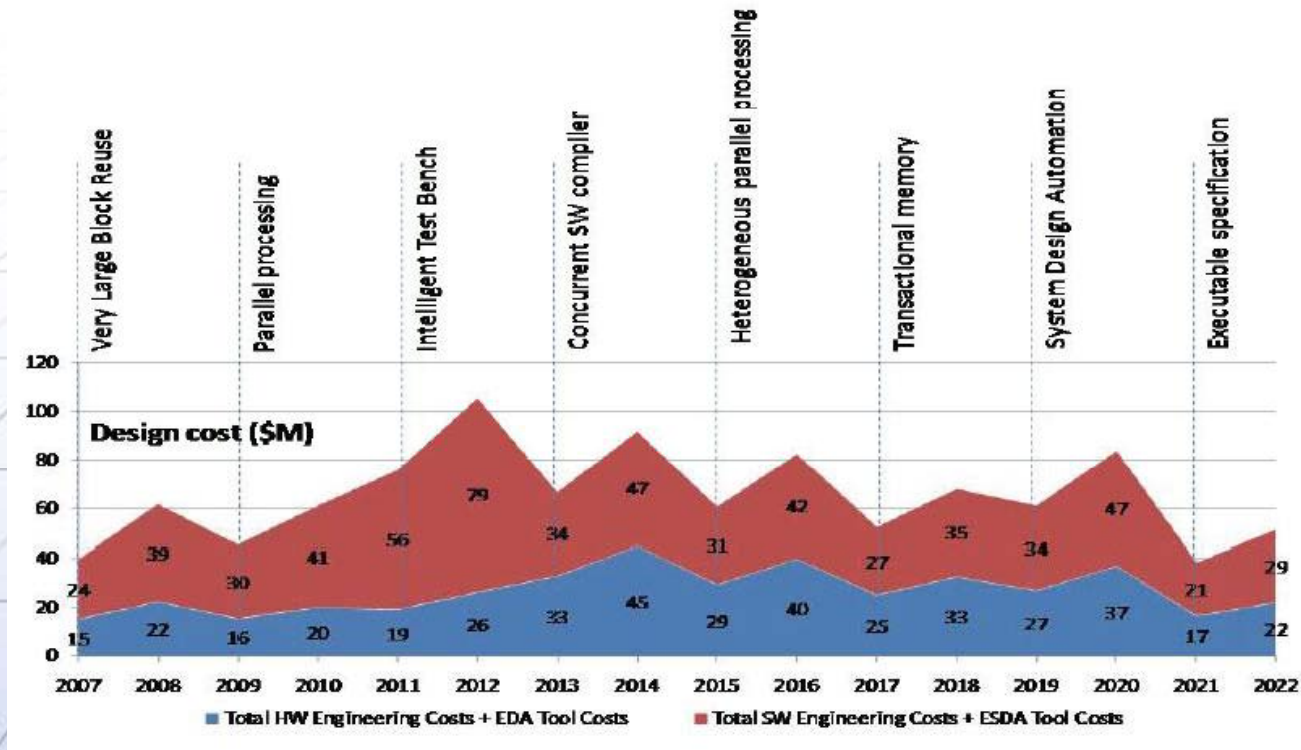


IBS Corp March '08

- **Test Cost**

- Reduction the cost of wafer test & final test
- To increase test coverage for large circuits
- To facilitate multi-site testing
- To use a low cost ATE

# Introduction



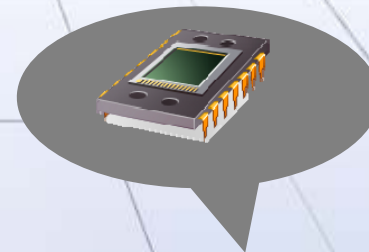
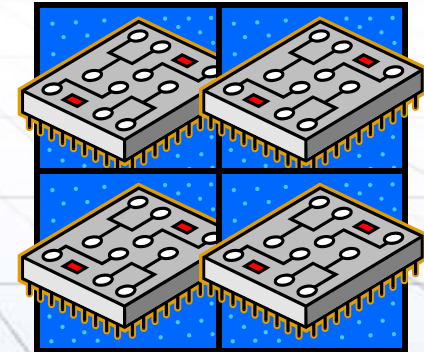
ITRS '07

- **Very large block reuse**
  - Many case HDL codes are modified for the test
  - Scan stitching & MBIST are inserted in top level
  - Hierarchical DFT flow is required

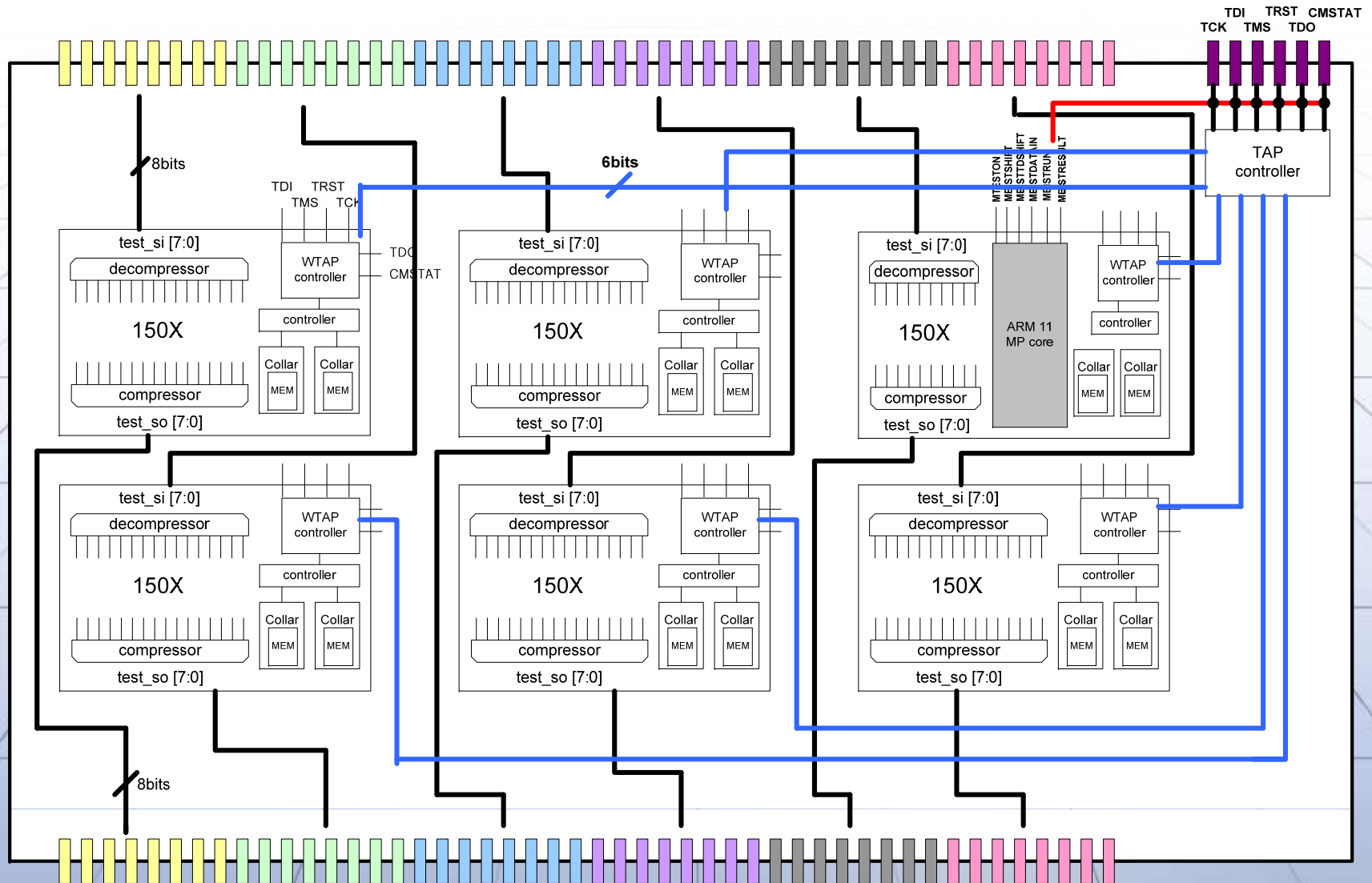
# Key factors for test cost reduction



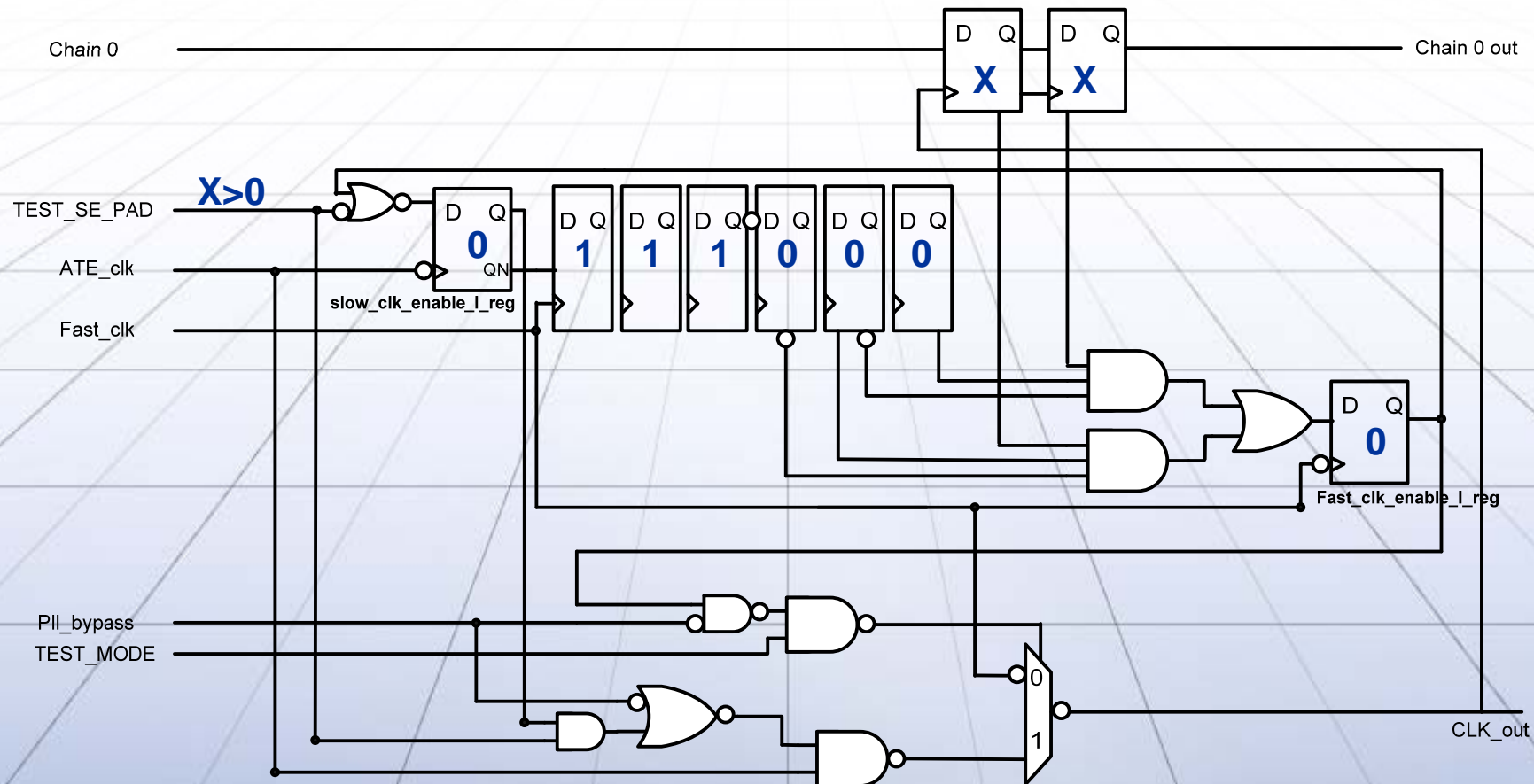
- **Test pattern volume**
  - ATE memory capacitance
  - Increasing test time
  - Multi DUT test
- **Low cost ATE**
  - Test cost saving per sec.
  - Load board cost
- **Test time**
  - Test cost saving each device
  - A number of test vectors are required
- **Reuse a large block**
  - Time-to-market



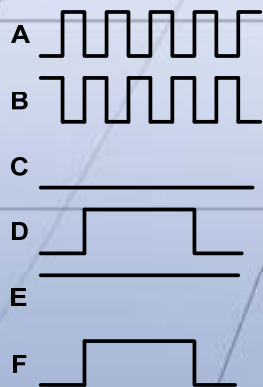
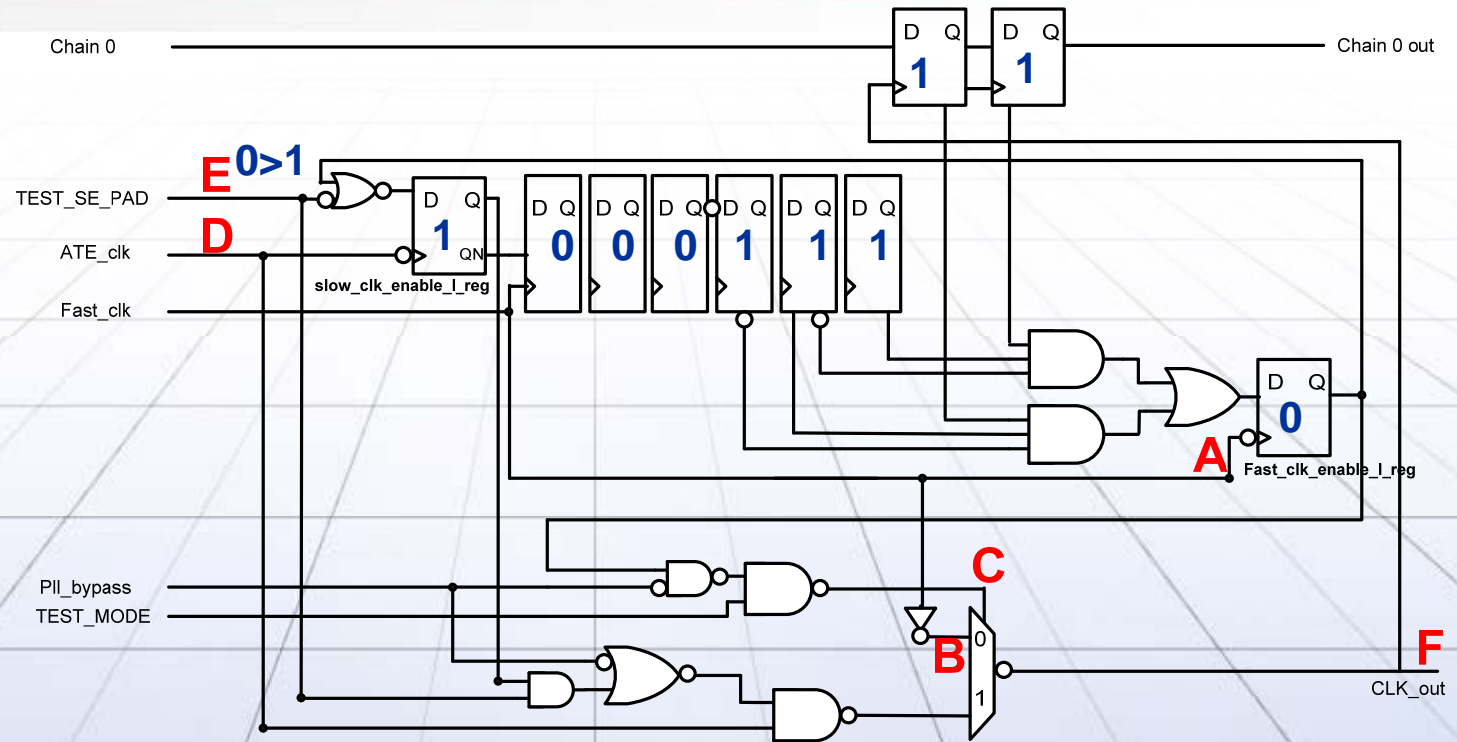
# Top block diagram within DFT



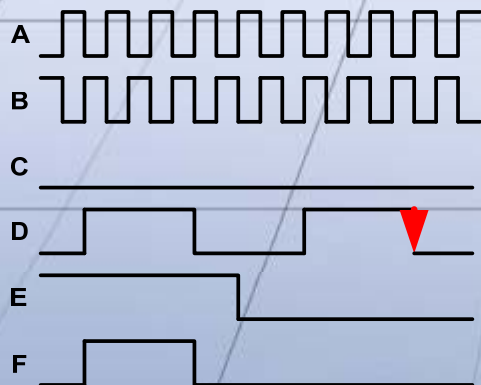
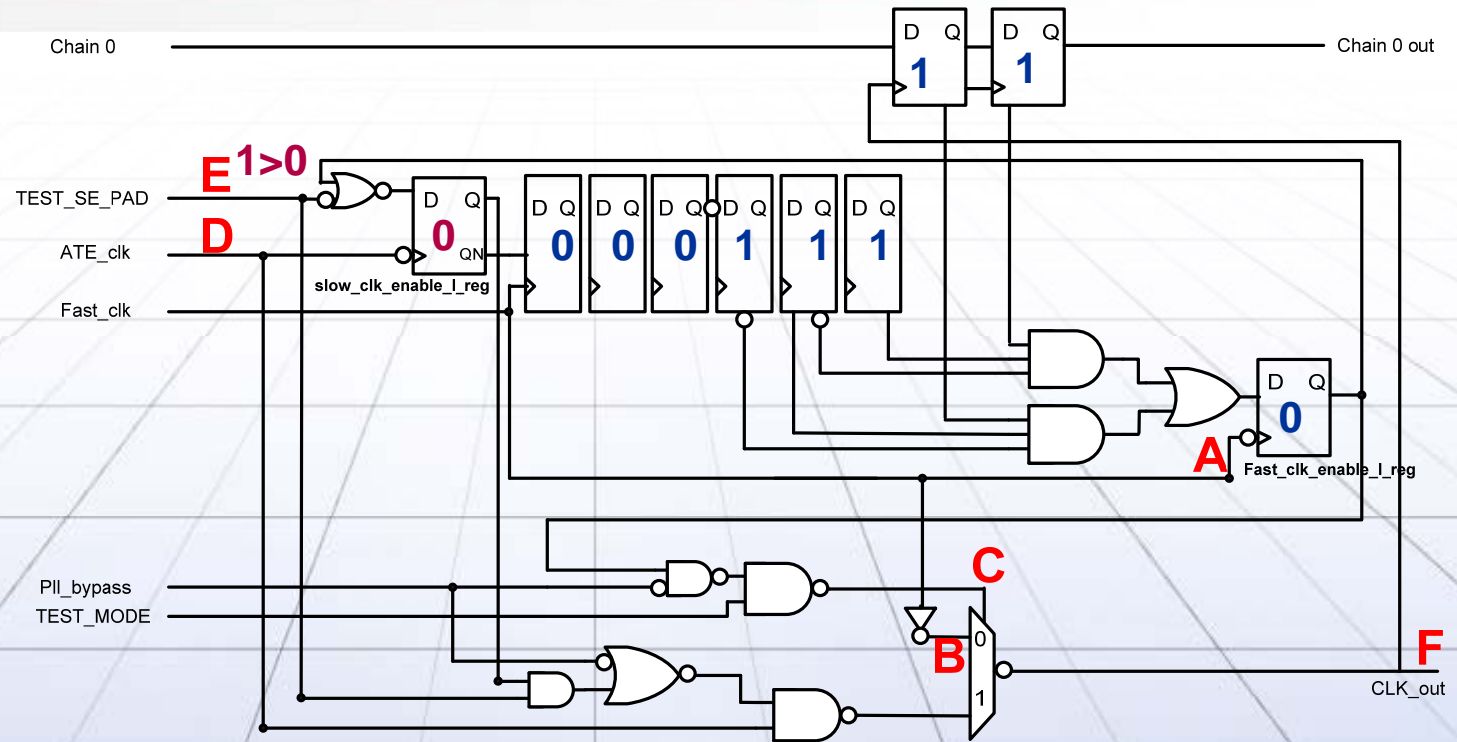
# OCC (On chip clocking) (1/9)



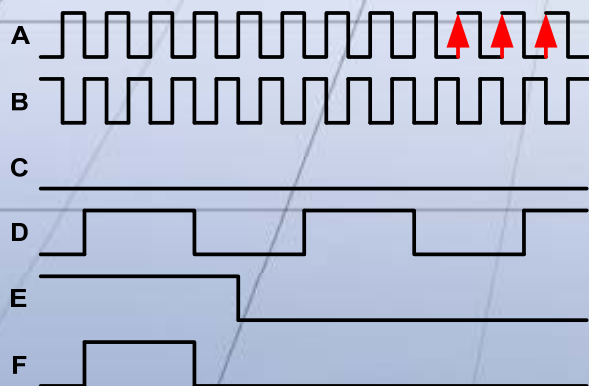
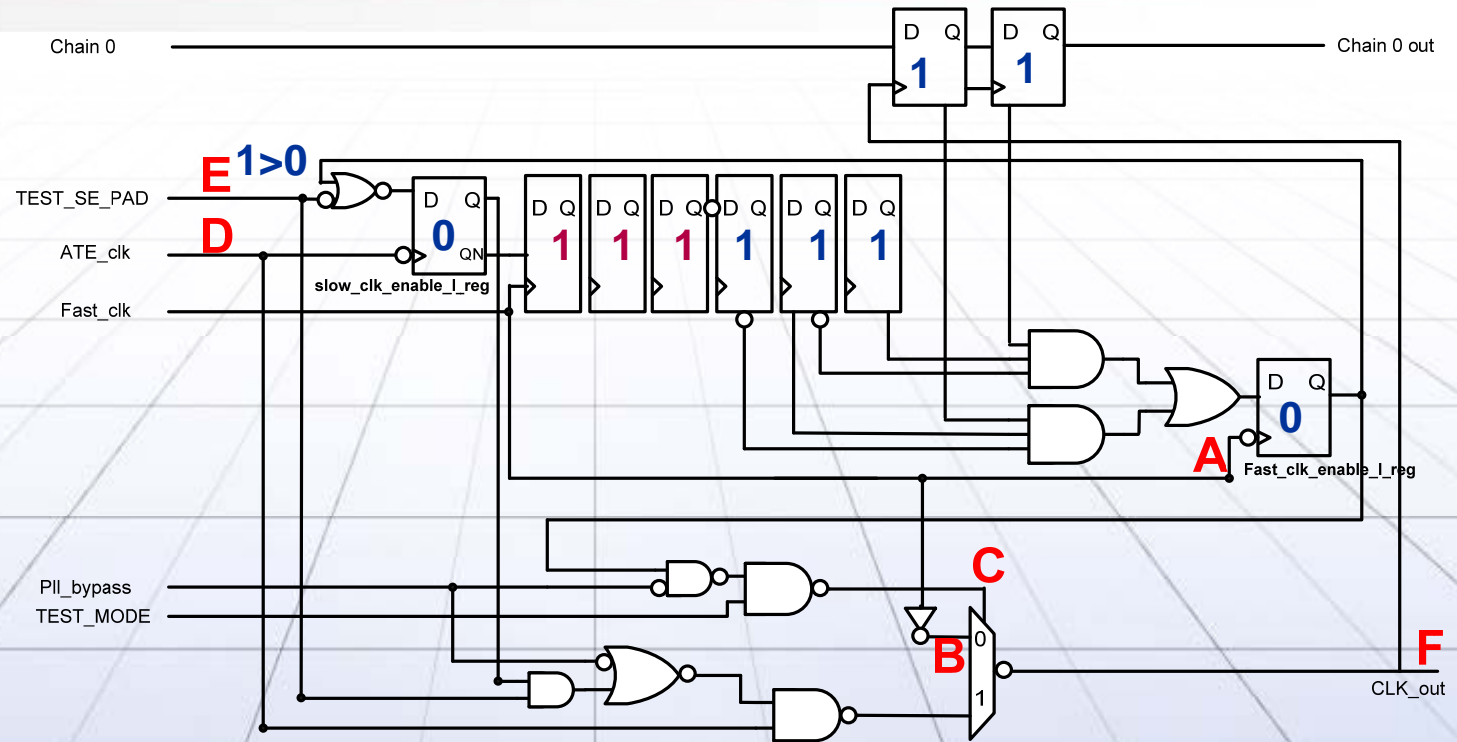
# OCC (2/9)



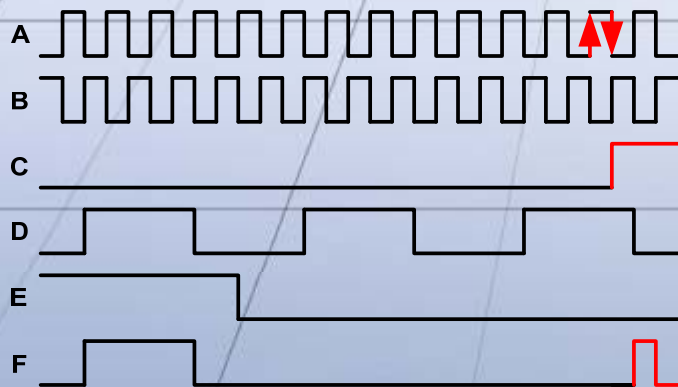
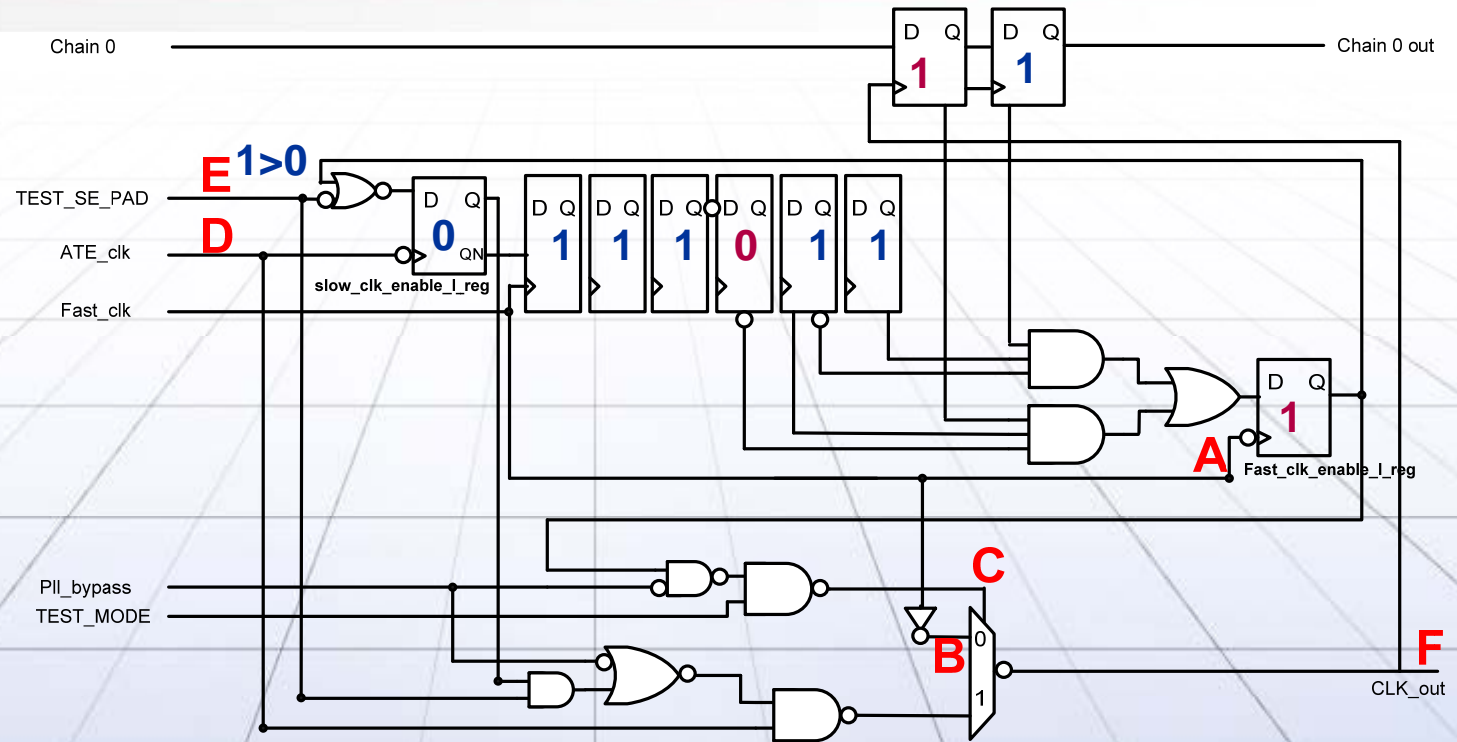
# OCC (3/9)



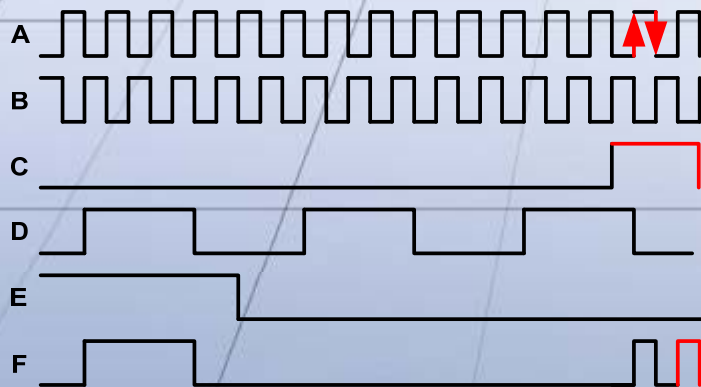
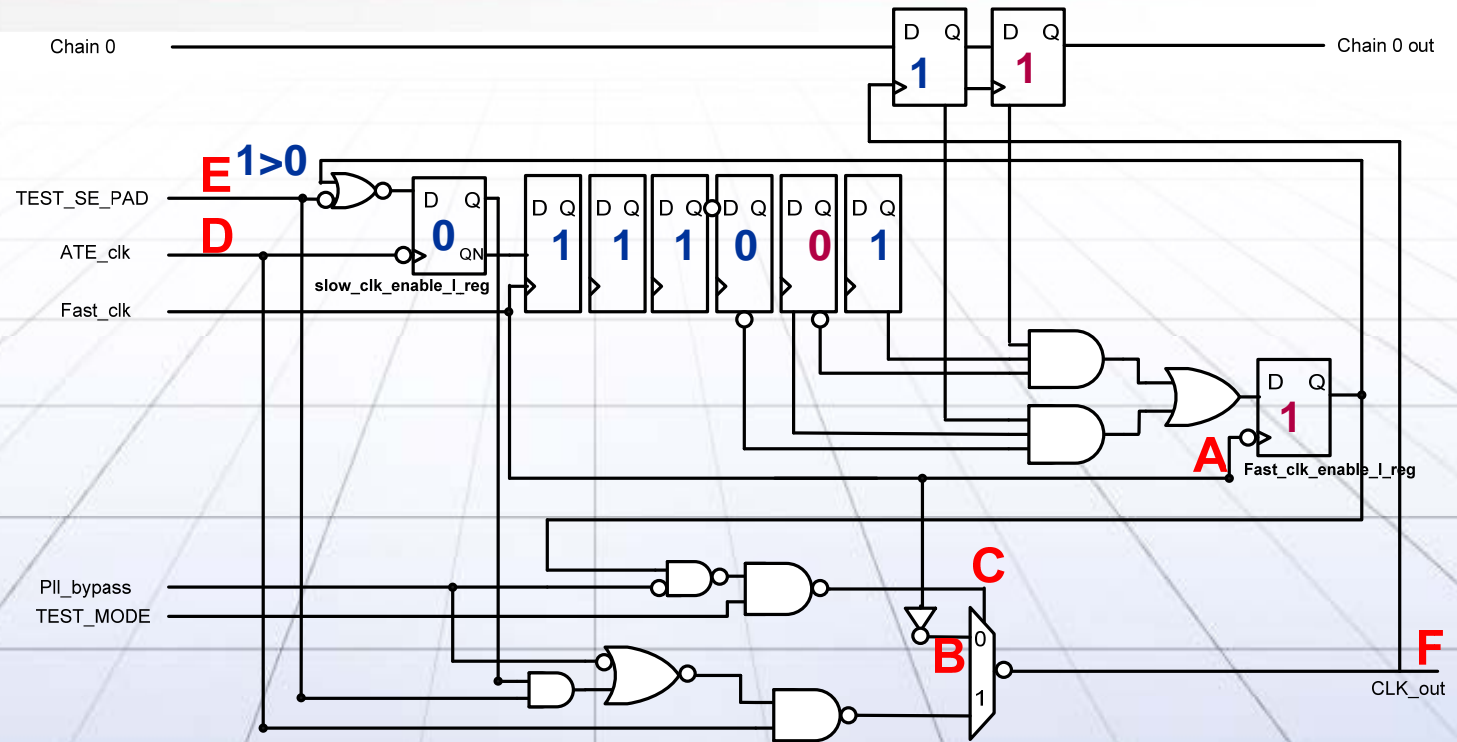
# OCC (4/9)



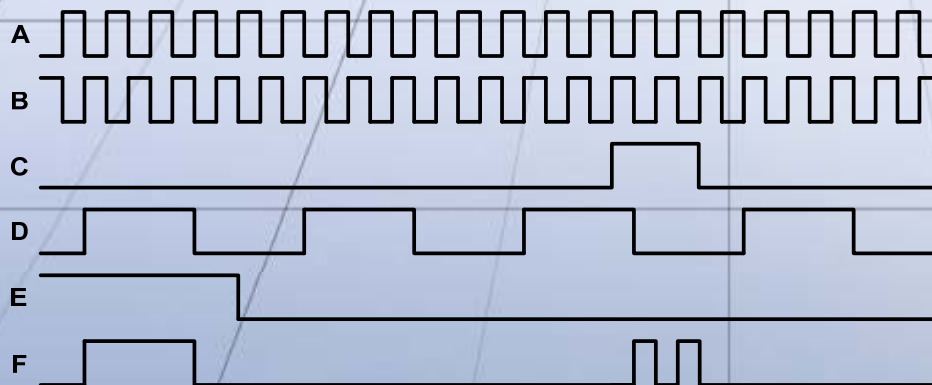
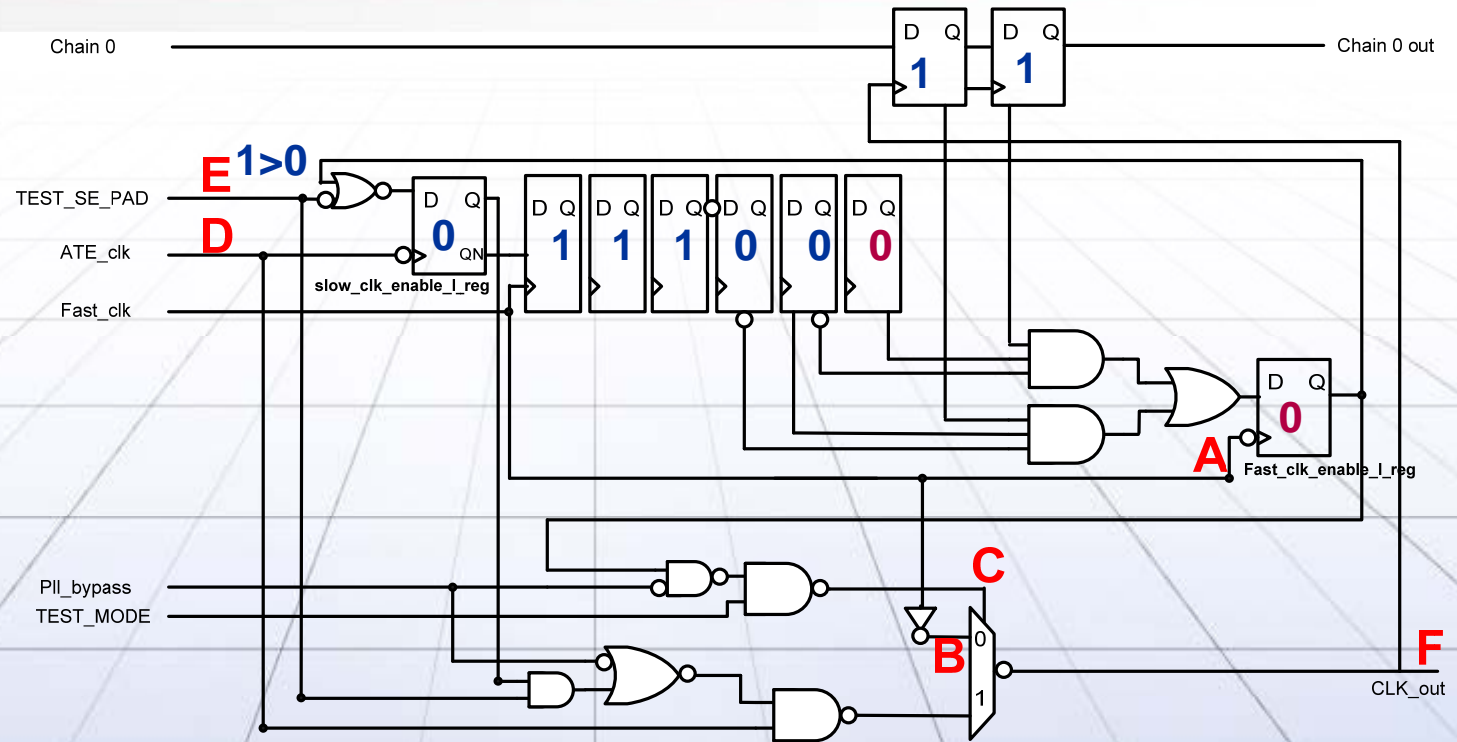
# OCC (5/9)



# OCC (6/9)

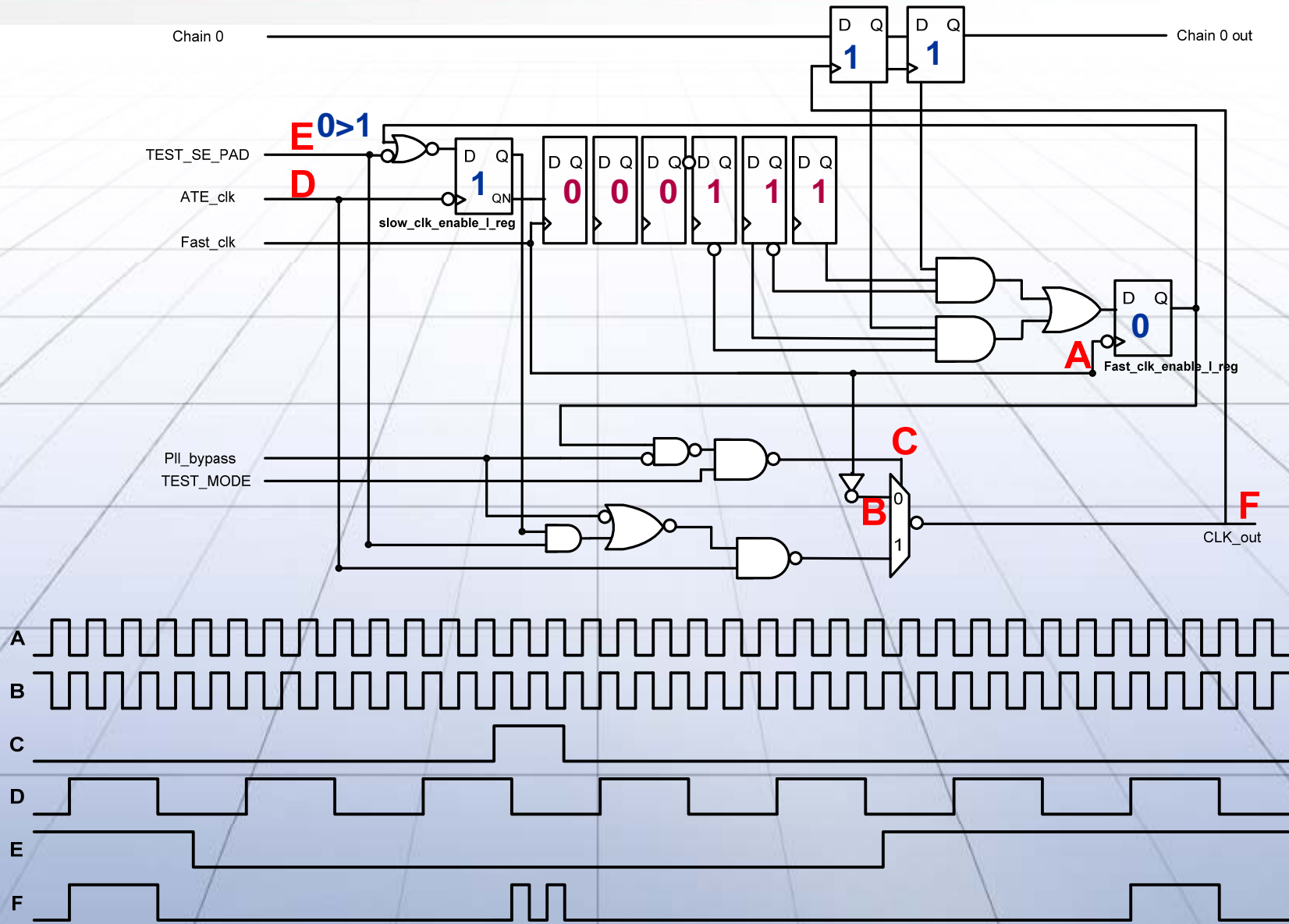


# OCC (7/9)

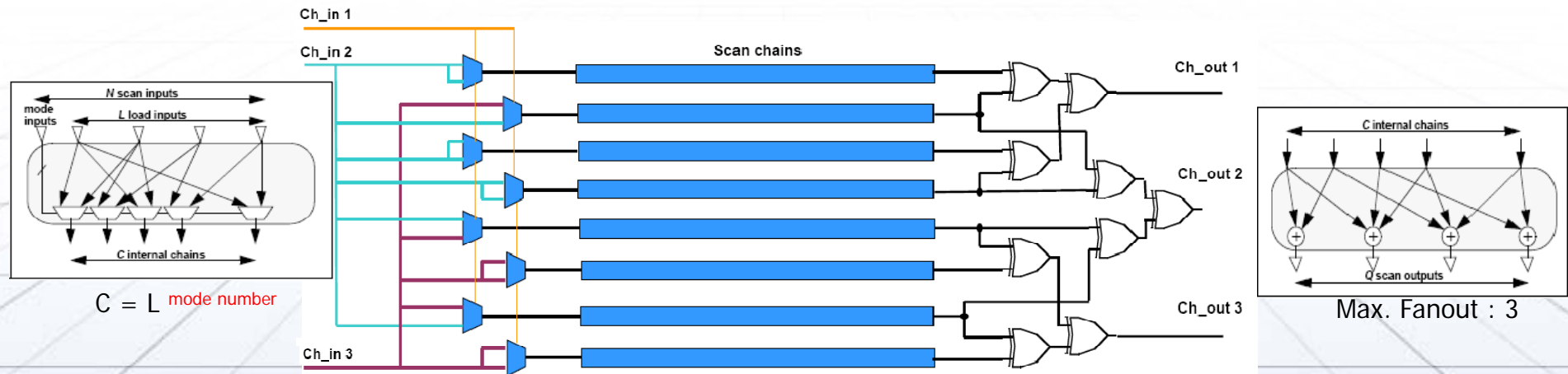




# OCC (9/9)



# Scan compression

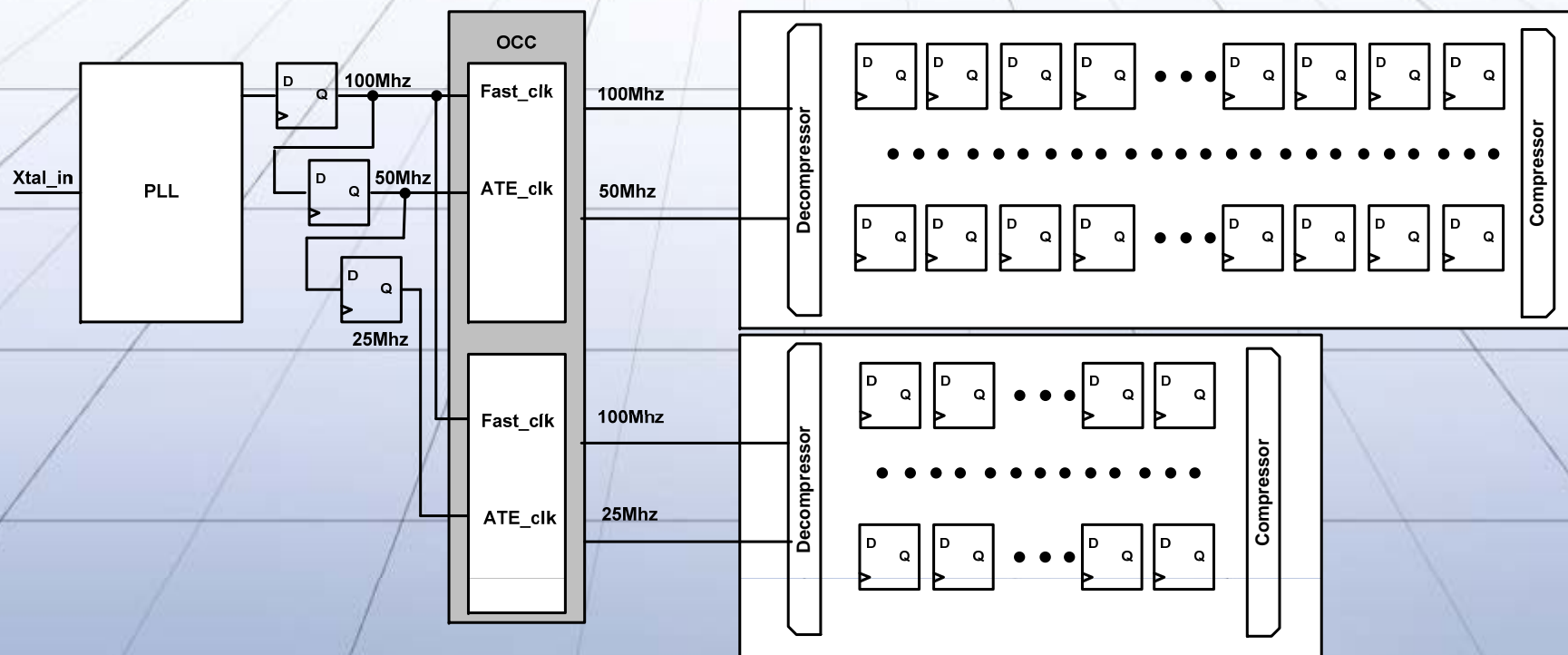


Synopsys DFT\_MAX

- **Key benefits**
  - 10-100x test time and test volume reduction to lower test costs
  - Same high test coverage and ease-of-use as standard scan
  - No impact on design timing
  - No impact on design physical implementation
  - Very low area impact
  - Tightly integrated with low-power design flows
  - Enables higher test quality for designs at 130-nm and below

# Scan balancing Method

- Calculate the block power for scan stitching in shift mode
- Compose of scan compression logics for each blocks
- Connect PLL & OCC & DFT block



# Scan STIL format



Scan shift frequency : 25Mhz

```
Timing {  
Period '50ns'  
50Mhz_clk { P { '0ns' D; '25ns' U; '50ns' ;D}}  
20Mhz_clk { P { '0ns' D; '25ns' U; '50ns' ;D}}  
}  
Pattern 0  
Chain1 {101010101...01010101010 }  
Chain2 {111011101...00000000000 }  
Pattern 1  
Chain1 {001010100...01111101010 }  
Chain2 {111010100...01100101010 }  
.....
```

Scan shift frequency : 50Mhz

```
Timing {  
Period '25ns'  
50Mhz_clk { P { '0ns' D; '14ns' U; '24ns' ;D}}  
25Mhz_clk { 01XZ { '0ns' }}  
}  
Pattern 0  
Chain1 {101010101...01010101010  
101010101...010101010}  
Chain2  
{11111100111110011...00000000000000000000  
}  
Pattern 1  
Chain1 {001010100...01111101010  
101110101...010111010}  
Chain2  
{111111001100110000...0011110000110011001100  
}  
.....
```

# Scan compression results



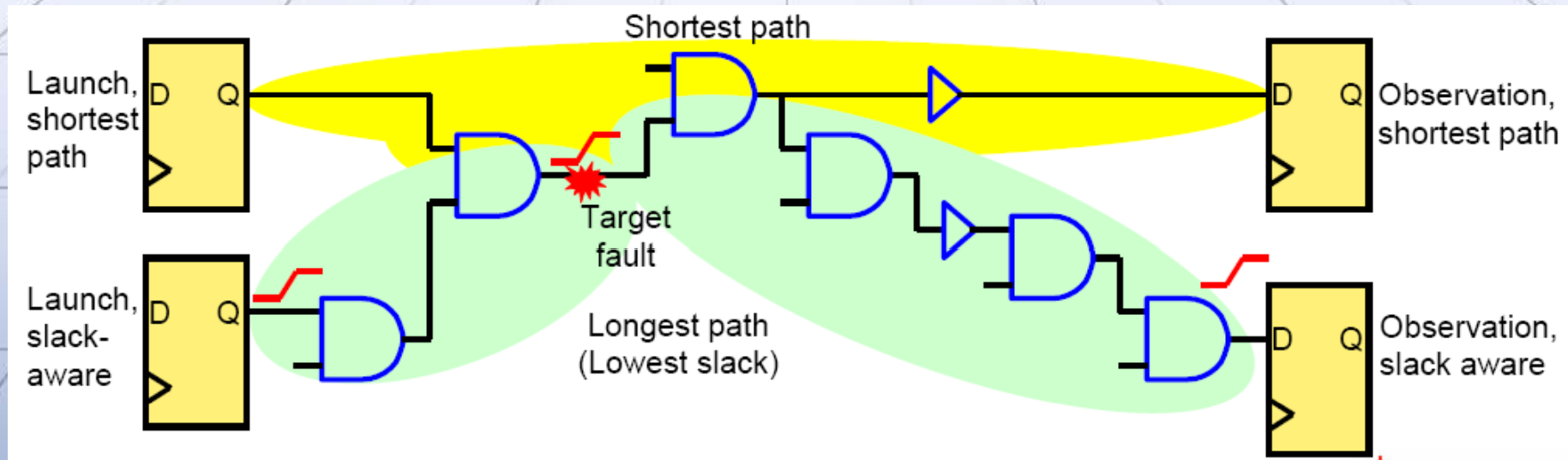
DUT	F/F (number)	scan chain	Gate count	Maximum Frequency / Test Clock Frequency
LGxxxx	268,925	16/160	17,143,112	400Mhz / 25Mhz

	Normal Scan	Scan compression	Scan balance Using scan compression
Scan chain /scan chain number	16chains 15100 FF	160chains 1510 FF	80chains (50Mhz) : 2012 FF 80chains (25Mhz) : 1006 FF
Test pattern volume	5,000 patterns * 15,100 length = 75,500,000	5000 patterns *1510 length = 7,550,000	5000 patterns * 2012 length = 10,060,000
Test coverage	Stuck-at fault : 99.4% Transition fault : 87.42%	Stuck-at fault : 99.4% Transition fault : 87.42%	Stuck-at fault : 99.4% Transition fault : 87.39%
Test time	3.41 sec	0.377 sec	0.252 sec
Hardware overhead	2.1%	2.4%	2.7%

# At-speed Test using SDD



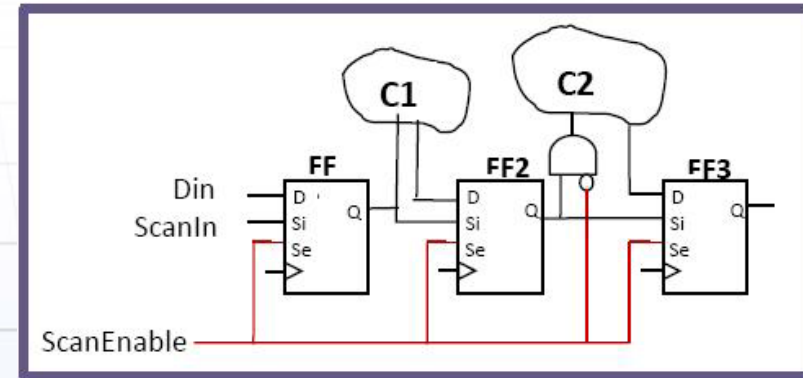
- Small Delay Defect (SDD) target faults and non-target faults
  - Uses slack-based test generation for defined SDD target faults
  - Uses regular transition fault test generation for all others in fault list
- Slack-aware tests detect small-delay defects
  - ATPG selects observation path with lowest slack
  - Slack data from timing sign-off tool



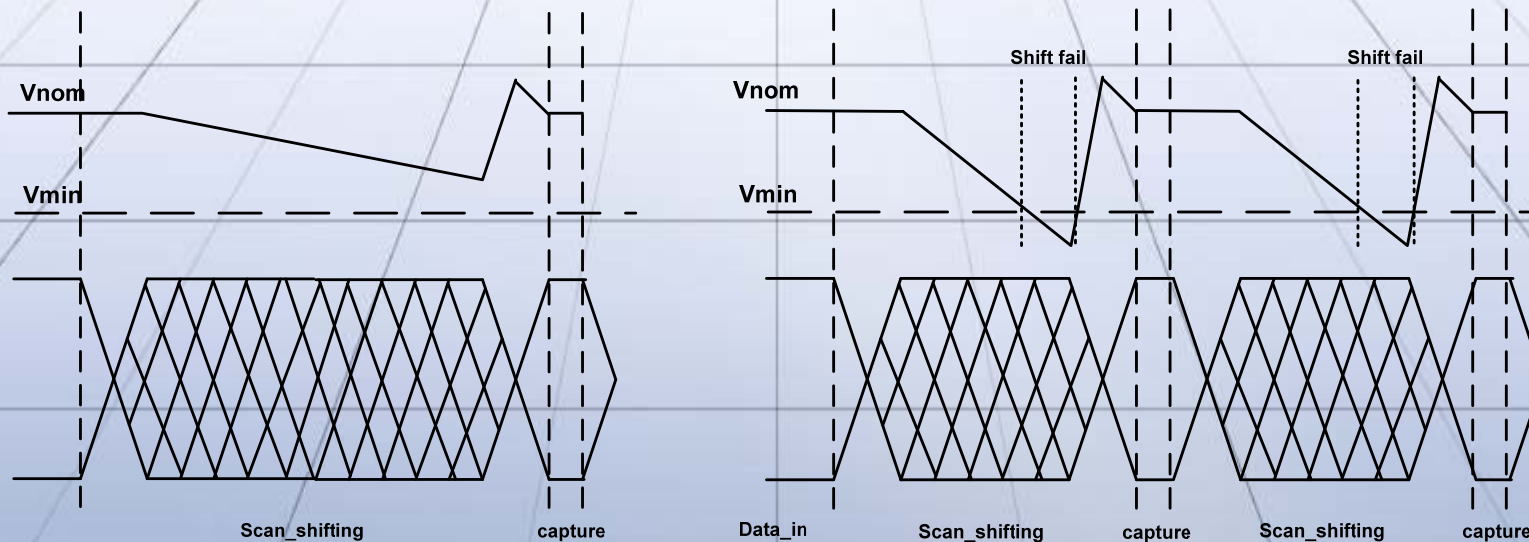
# Power-aware DFT



- **Power-aware DFT using AND gate**
  - Logic driven by the functional output does not toggle during scan shift
  - Adds an AND gate at the functional output of a scan flop per user's specification
- **Benefit**
  - Reduces power dissipation during shift

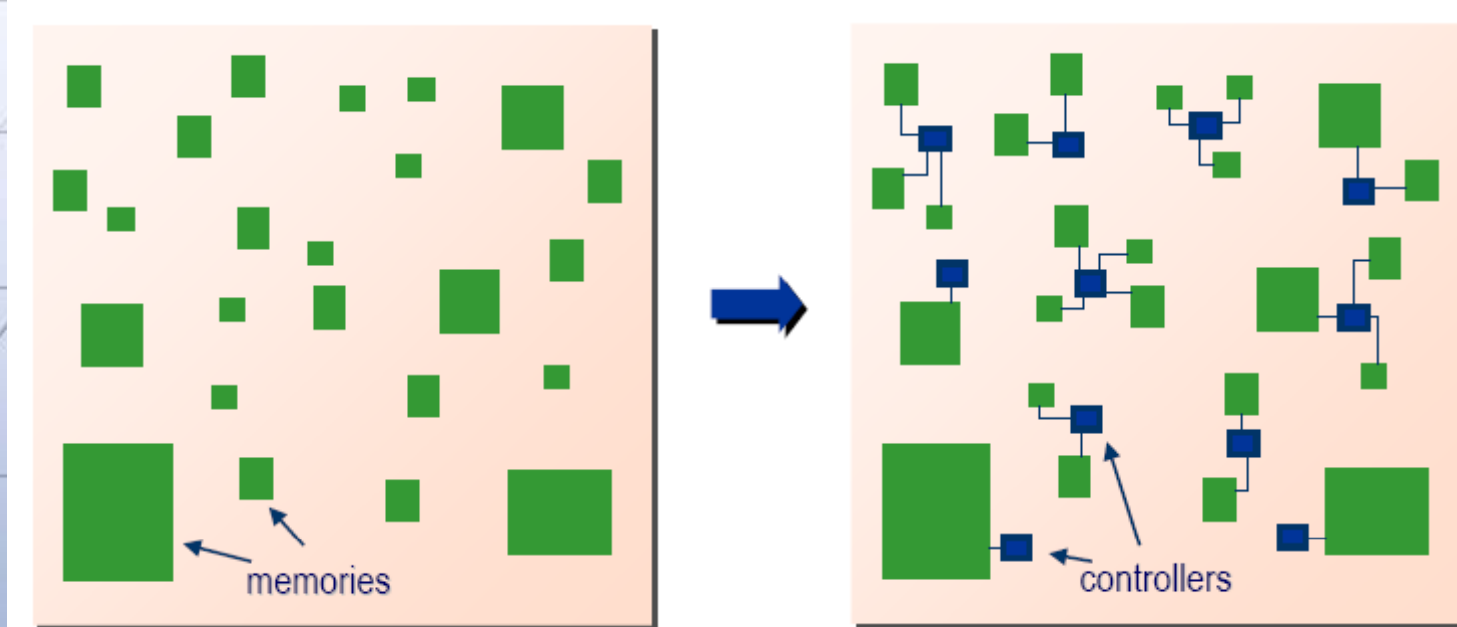


Synopsys DFT\_Compiler

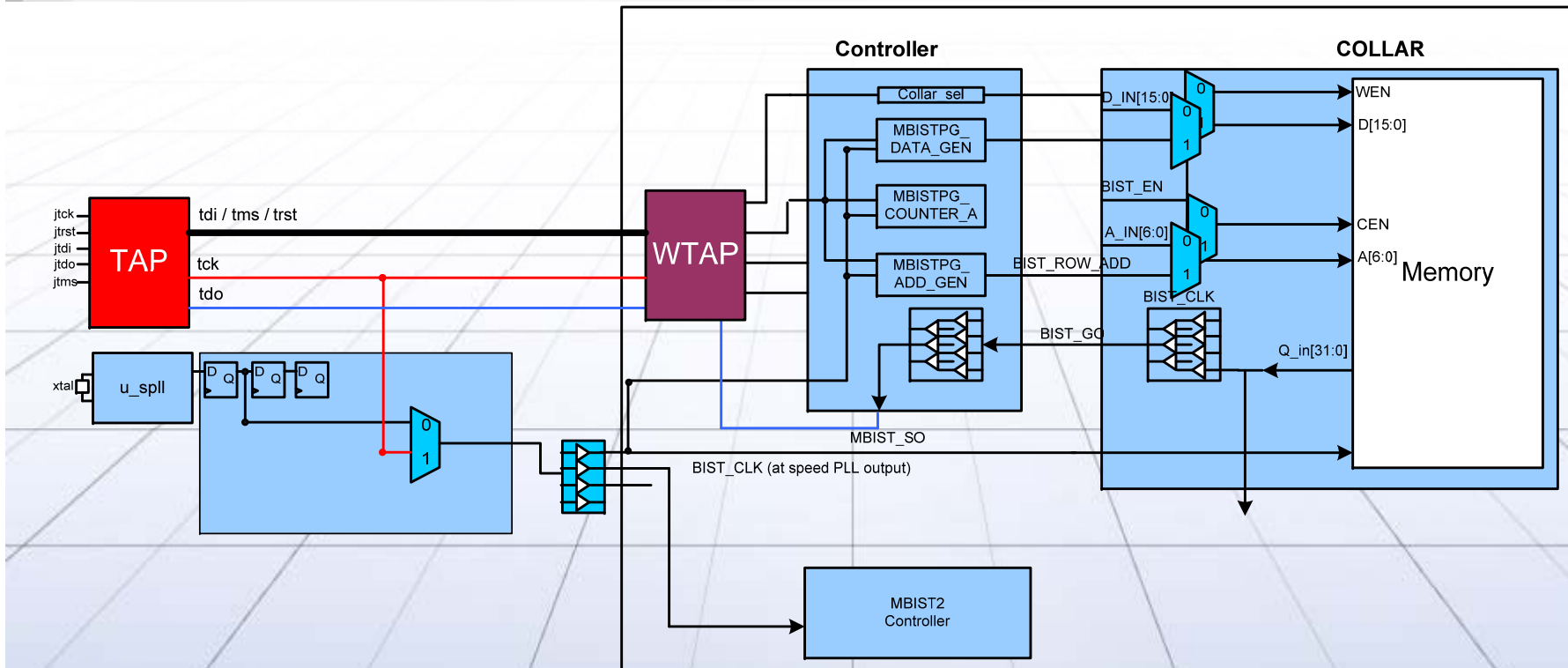


# MBIST using PLL clock source

- **Controllers configured and assigned to memories based on several criteria / constraints including**
  - Clock domains
  - Physical clustering
  - Test time
  - Power draw



# MBIST detail connection



Mentor Graphics

**Test time of Algorithms :  $20N + 2 * \text{retention time}$**   
 (determined by retention time in the memory library file)

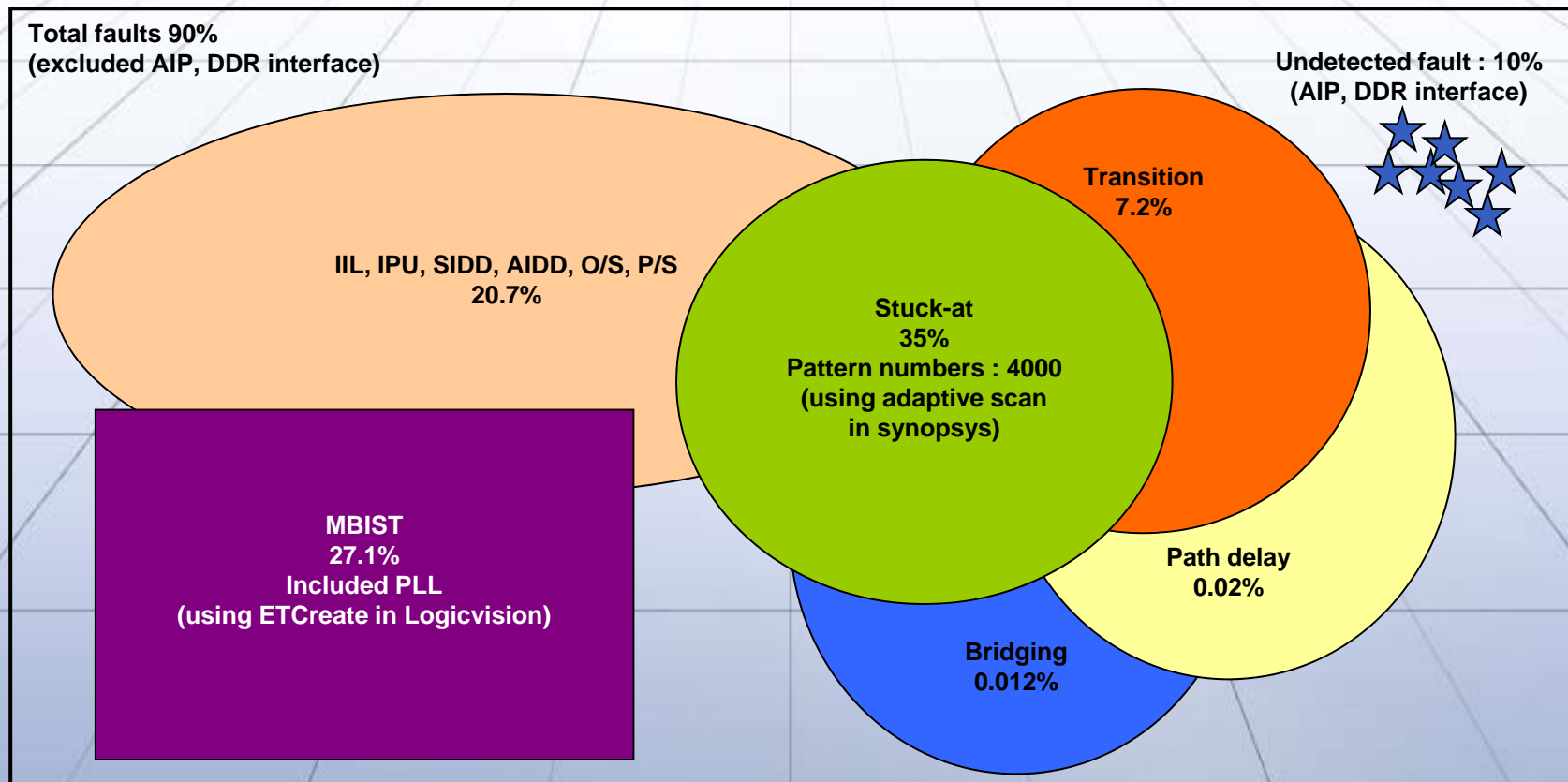
**Fault model list :** Stuck-at faults \* Transition faults \*  
 Unlinked dynamic coupling faults \* Address decoder faults \*  
 Read/Write logic faults \* Parametric faults  
 ( cycle time, write recovery time, data retention )  
 Destructive read faults \* Single-port bitline coupling fault

# Fault Summary Report (Wafer test)

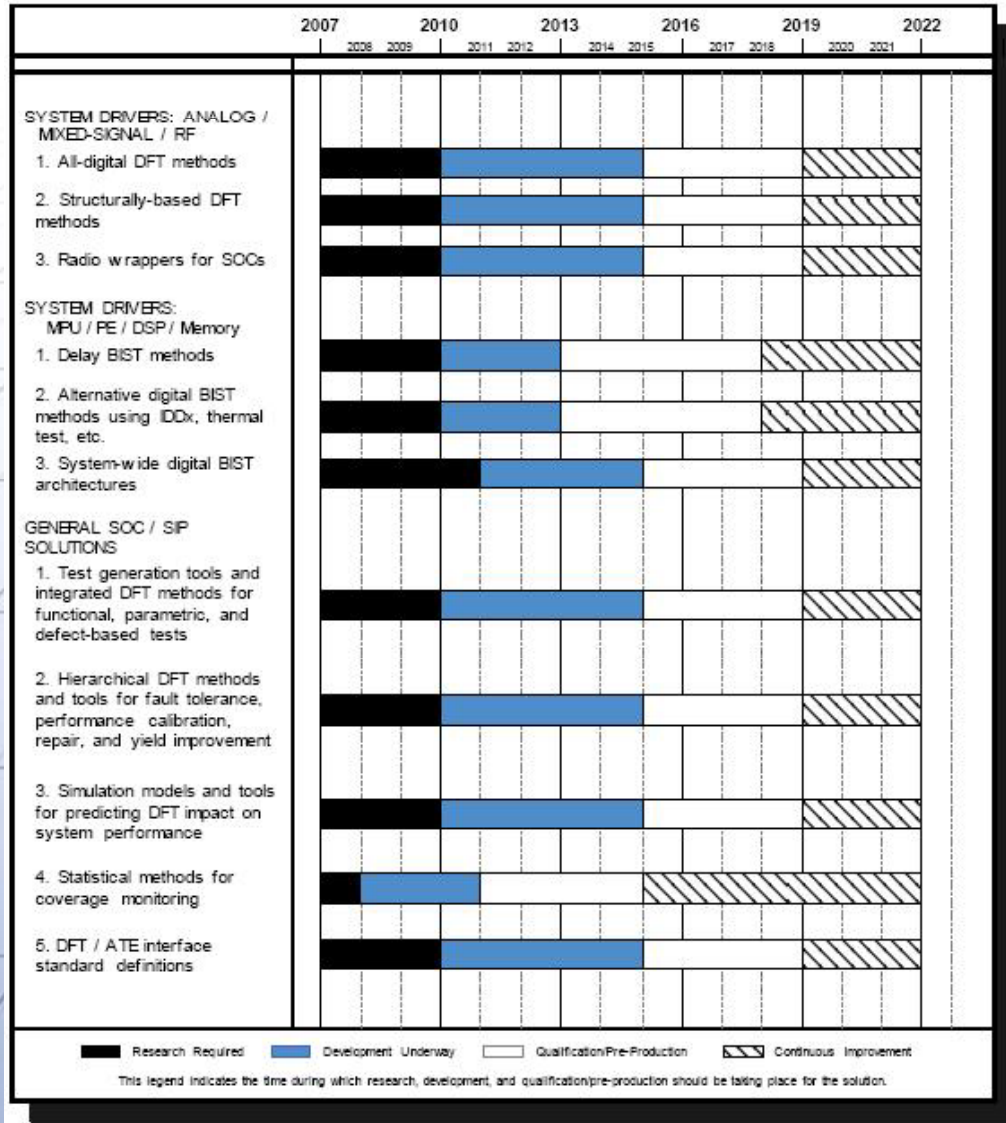


	O/S	P/S	IIL	IPU	IIL	SIDD	AIDD	MBIST	SCAN	SC_TR	SC_PATH	SC_BR
Per input	0.044%	0.270%	0.019%	0.000%	0.016%	0.262%	0.022%	0.840%	1.065%	0.222%	0.001%	0.000%
Per fail	1.602%	9.766%	0.689%	0.000%	0.576%	9.496%	0.811%	30.427%	38.571%	8.031%	0.020%	0.012%

- \* path delay pattern is covered 10ppm
- \* Bridging pattern is covered 5~6ppm
- \* TSMC 65nm LP process



# Future Works



- **Analog / Mixed-signal / RF**

- All-digital DFT methods
- Structurally-based DFT methods
- RF wrappers for SoCs

- **MPU / PE / DSP / Memory**

- Delay BIST methods
- Alternative digital BIST methods using IDDx, thermal test, etc.
- System-wide digital BIST architectures

- **SoC / SIP solutions**

- Test generation tools and integrated DFT methods
- Hierarchical DFT methods
- Simulation models and tools for predicting DFT impact on system performance
- Statistical methods for coverage monitoring
- DFT / ATE interface standard definitions