DFT Methodology for Power Issues during Production Test

Beom Ik, Cheon
bi.cheon@samsung.com
Nov. 15, 2008

Design Technology Team
System LSI, Samsung Electronics
Contents

- Introduction
- Power-aware DFT Design
- Power-Aware ATPG
- DFT Implementation Flow
- References
Test Issues for SOC Devices with Large Size

- Test Cost
  - Test Time
  - Test Data Volume

- Quality
  - Defect PPM
  - Fault Model

- Yield
  - Overkill
  - Yield Loss due to Power during Production Test
Power-aware Test Challenge

- Power-aware DFT Design
  - DFT Design w/o Power Design
  - Power Reduction during Test
- Power Design and Analysis
  - Si Overhead
  - Static Power Analysis
  - Dynamic Power Analysis
- Solutions for Power-aware DFT
  - DFT Design
    - Power Scheduling
    - Power Management
  - ATPG
    - Low Power Budget
Power Reduction for Scan Test Mode

- Design Modification
  - Scan Chain Ordering
  - Gating Blocking
  - Design Partitioning

- Test Pattern Generation
  - Test Pattern Modification
  - Test Pattern Compression
  - Test Pattern Ordering
  - Power-aware ATPG
Test Power Estimation

- **WSA (Weighted Switching Activities)**
  - S1: Constraints at Each Node
    - Toggles at Each Node
    - No of Fan-out of Each Node
  - S2: Constraints at Each Flip-Flop
    - Toggles at Each Flip-Flop
  - S3: Constraints at Each Flip-Flop
    - Toggles at Each Flip-Flop
    - Fan-out Cone Size of Each Flip-Flop

Scan-in power estimation

2008 Test Workshop [5]
Contents

- Introduction
- Power-aware DFT Design
- Power-Aware ATPG
- DFT Implementation Flow
- References
Power-aware Scan Chain Ordering

V1 = 0 1 1 0  R1 = 0 1 0 0
V2 = 0 1 0 1  R1 = 1 0 0 0
V3 = 0 1 1 1  R1 = 1 0 1 1

Weight Transitions = \( \Sigma \) (Size of Scan Chain Position Transition)

Power-driven scan chain routing on circuit 9234 without routing constraint
Scan Chain Ordering with Routing Constraints

- Clustering
- Power-driven Scan Cell Reordering after ATPG
- Cluster Ordering

Drawbacks
Gate Blocking

- Power Reduction during Shift Mode
  - FF Output Signal Disable
  - FF with Low Activity

- Drawbacks

Scan path element with reduced output activity
Design Partitioning

- Design Partition with Clock Gating
  - How to partition the device?
    - Test Time
    - Fault Coverage

- Drawbacks

![Diagram of scan chain and gated sub-chains]
Design Partitioning

- Design Partition with Multiple Scan Enable Signals
  - How to partition the device?
    - Test Time
    - Fault Coverage

- Drawbacks

A diagram illustrating the hierarchical scan implementation with constant data inputs.
Design Partitioning

- MD-SCAN (multi-duty scan)
  - How to decide the duty depth?
  - Different clock for shift and capture mode

- Drawbacks
Contents

- Introduction
- Power-aware DFT Design
- Power-Aware ATPG
- DFT Implementation Flow
- References
Test Pattern Modification

- Random X-Filling
  - Dynamic compaction for detecting more faults

- Non-Random X-Filling
  - 0-Filling
  - 1-Filling
  - Adjacent X-Filling

A histogram of the fraction of care bits in deterministic scan patterns for Module M.
Test Pattern Modification

- LCP (Capture Power Reduction) X-Filling
  - Issues
    - Target Selection Problem
    - Value Selection Problem
  - Methods
    - 0-Filling, 1-Filling, Minimum-Transition-Filling
      - w/o considering the Impact of Capture Power
    - X-Filling for Reduction of Logic Transition Count at Scan FF outputs.
      - No Correlation with total Capture Power and Scan FF Transition

\[ \begin{array}{cccccccccc}
  X & 1 & X & X & X & 0 & X & X & X & X & 1 \\
\end{array} \]

(1) target selection
(2) value selection (0/1)
LCP X-Filling

- LCP X-Filling
  - X-Score for *X-Filling Target Selection*
  - Probabilistic Weighted Capture Transition Count for *X-Filling Value Selection*
    - The probabilistically-estimated number of weighted capture transitions at all nodes (gates and FFs)
    - Weight:
      - Toggles
      - Fan-out cone size

Weighted capture transition count: (G1, G3, ff1)

\[ WCT(v1) = 1*1 + 1*1 + 1*2 = 4 \]
Test Pattern Modification

Test Pattern Modification with Bit-Stripping

- Original Scan Vector: 1 0 0 1 0 1 1 0 1 0 1 0 0 1 0 1 1 0
  (13 transitions)
- After Bit-Stripping: X X 0 1 X 1 X 0 1 0 X X X 1 0 0 1 1 X
- After MT-Fill: 0 0 0 1 1 1 1 0 1 0 0 0 1 0 0 1 1 1
  (7 transitions)
Test Pattern Compression

- Static Compaction considering Power Dissipation
  - Constraint WSA (Weighted Switching Activities)

\[ V_1 = \times 0 \times 0 \times 0 \times \]
\[ V_2 = 1 \times 1 \times 1 \times 1 \times 1 \]

(6 Transition)

\[ V_0 = 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \]
Power-aware ATPG

- Low Power for Capture Mode

Conventional ATPG

Vectors with High Capture Power ($T_v$) is replaced with new Vectors (low capture power)

Fault List Generation for $T_v$

Capture-power aware ATPG

Concept of Overlapping Degree.
Contents

- Introduction
- Power-aware DFT Design
- Power-Aware ATPG
- DFT Implementation Flow
- References
Power-Aware Scan Design & ATPG Flow

Scan Design

Conventional ATPG

Remove ATPG pattern with high Switch Activity

Power-aware ATPG

Power-ware ATPG

Conventional ATPG

Vector frequency

Switching Activity

power-critical patterns
Power-Aware Scan Design & ATPG Flow

Scan Design

→

Power-aware ATPG

→

Remove ATPG pattern with high Switch Activity

→

Conventional ATPG

Diagram:

- Combinational Portion
- Conventional ATPG
- Power-ware ATPG
- Vector frequency
- Switching Activity
Power-Aware Scan Design & ATPG Flow

1. Power-aware Scan Design
2. Power-aware ATPG
3. Remove ATPG pattern with high Switch Activity
4. Conventional ATPG
5. Correlation with Shmoo
6. Power-aware ATPG With design constraints

Power-ware ATPG

Conventional ATPG

Switching Activity

power-critical patterns
Power-Aware Scan Design & ATPG Flow

1. Power-aware Scan Design
2. Power-aware ATPG
3. Remove ATPG pattern with high Switch Activity
4. Conventional ATPG
5. Correlation with Shmoo
6. Power-aware ATPG With design constraints

Diagram:
- Power-ware ATPG
- Conventional ATPG
- Vector frequency
- Switching Activity
- Power-critical patterns

2008 Test Workshop [24]
ATPG & Power Issues with Memories

- Power issue of memories for ATPG
  - ATPG w/ memories
    - Algorithm
    - Test time
    - Fault coverage
    - Test quality
  - ATPG w/o memories
    - Memories: black box
    - Memories are disabled
**Example of Power-Aware Scan Design & ATPG Flow**

1. **RTL Code**
   - Scan Design Rule Check (1)
   - Fault Coverage Estimation (2)
   - Synthesis (3)
   - Power-aware Scan Design with Scan Compression (4)

2. **ATPG with Switch Activity Budget** (5)
   - Remove ATPG pattern with high FF Switch Activity (6)
   - Enough FC? (7)
     - yes
     - ATPG with Switch Activity Budget and design partitioning (8)
     - Remove ATPG pattern with high FF Switch Activity (9)
     - Enough FC? (10)
       - yes
       - Conventional ATPG (11)
       - Finished (12)
       - Shmoo Analysis (13)
       - Remove ATPG pattern with power issue (14)
       - Add test patterns for target faults (15)

3. **WSA**

4. **X-Filling**
   - Bit-Stripping
   - Static Compression
   - Power-aware ATPG

---

**High Fault Coverage with Low Overhead**

**Scan Chain Ordering**
- Gating Blocking
- Design Partitioning

**Si Correlation with Shmoo**

---

**2008 Test Workshop [26]**
References


