

DFT Methodology for Power Issues during Production Test

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- **Introduction**
- Power-aware DFT Design
- Power-Aware ATPG
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- References

Test Issues for SOC Devices with Large Size

■ Test Cost

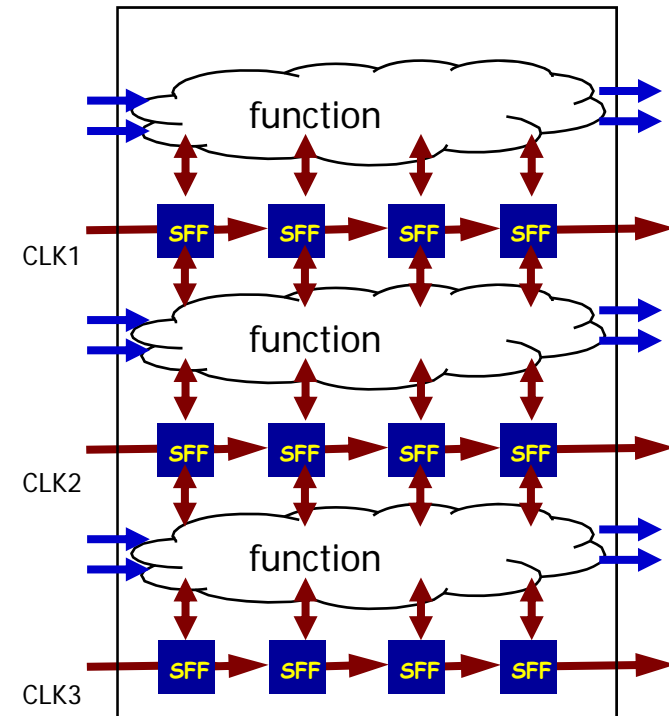
- Test Time
- Test Data Volume

■ Quality

- Defect PPM
- Fault Model

■ Yield

- Overkill
- Yield Loss due to Power during Production Test



Power-aware Test Challenge

■ Power-aware DFT Design

- DFT Design w/o Power Design
- Power Reduction during Test

■ Power Design and Analysis

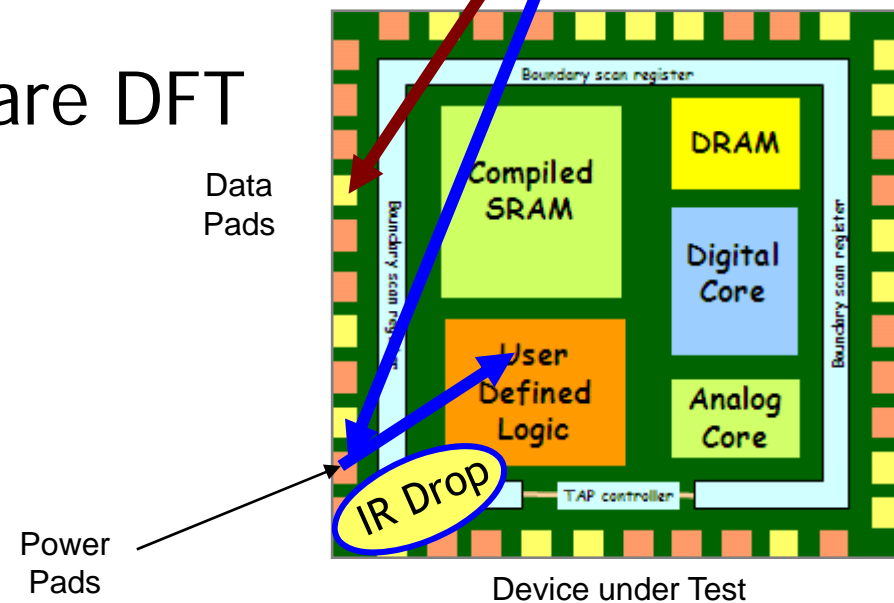
- Si Overhead
- Static Power Analysis
- Dynamic Power Analysis

■ Solutions for Power-aware DFT

- DFT Design
 - ◆ Power Scheduling
 - ◆ Power Management
- ATPG
 - ◆ Low Power Budget

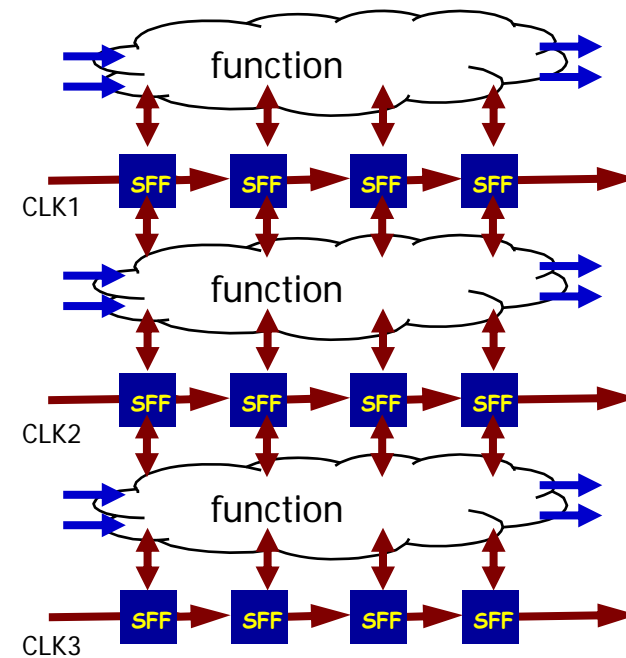


Power Supply



Power Reduction for Scan Test Mode

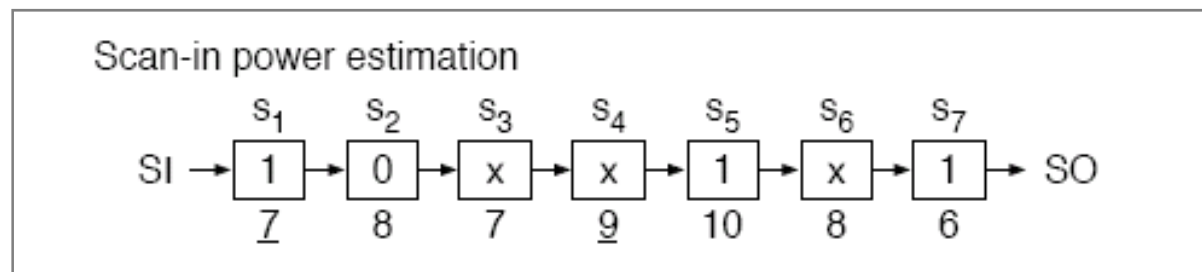
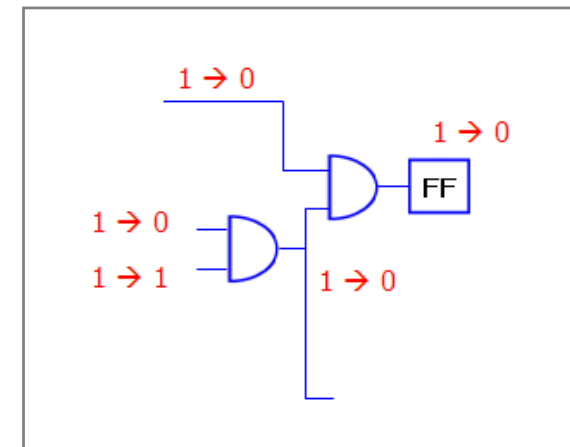
- Design Modification
 - Scan Chain Ordering
 - Gating Blocking
 - Design Partitioning
- Test Pattern Generation
 - Test Pattern Modification
 - Test Pattern Compression
 - Test Pattern Ordering
 - Power-aware ATPG



Test Power Estimation

■ WSA (Weighted Switching Activities)

- S1: Constraints at Each Node
 - ◆ Toggles at Each Node
 - ◆ No of Fan-out of Each Node
- S2: Constraints at Each Flip-Flop
 - ◆ Toggles at Each Flip-Flop
- S3: Constraints at Each Flip-Flop
 - ◆ Toggles at Each Flip-Flop
 - ◆ Fan-out Cone Size of Each Flip-Flop



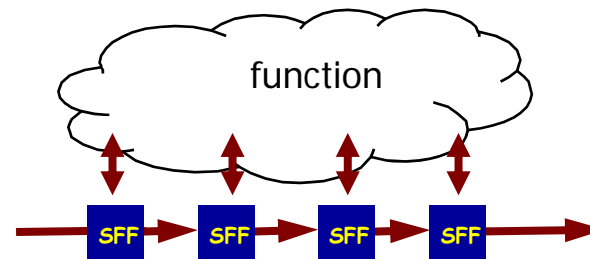
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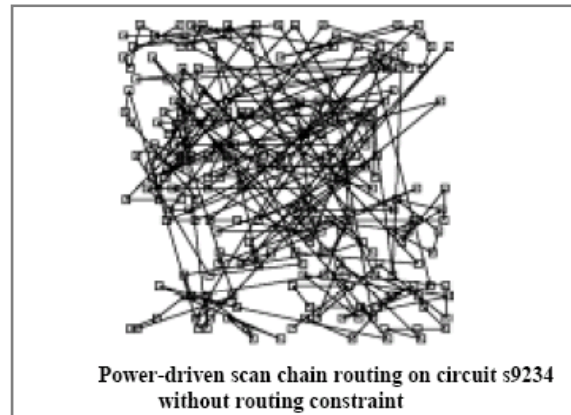
Power-aware Scan Chain Ordering

■ Power-aware Scan Chain Ordering

V1 = 0 1 1 0	R1 = 0 1 0 0
V2 = 0 1 0 1	R1 = 1 0 0 0
V3 = 0 1 1 1	R1 = 1 0 1 1

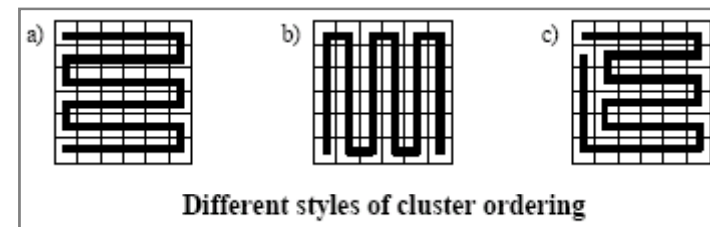
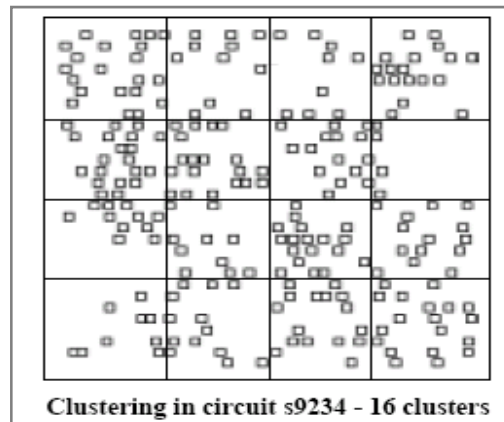
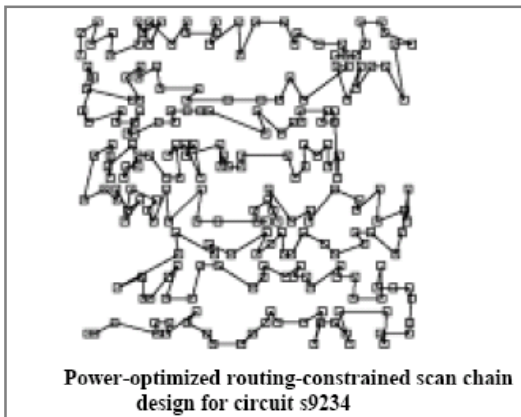
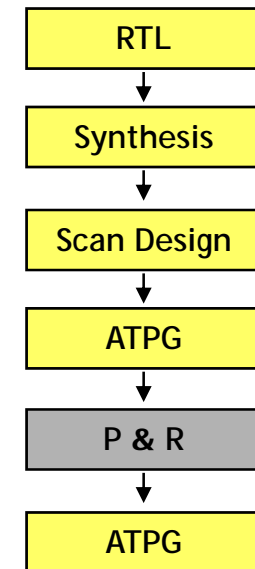


Weight Transitions = Σ (Size of Scan Chain Position Transition)



Power/Routing-aware Scan Chain Ordering

- Scan Chain Ordering with Routing Constraints
 - Clustering
 - Power-driven Scan Cell Reordering after ATPG
 - Cluster Ordering
- Drawbacks

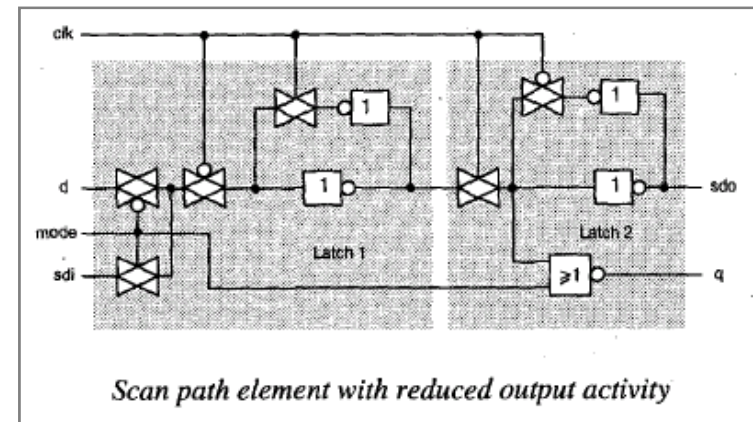
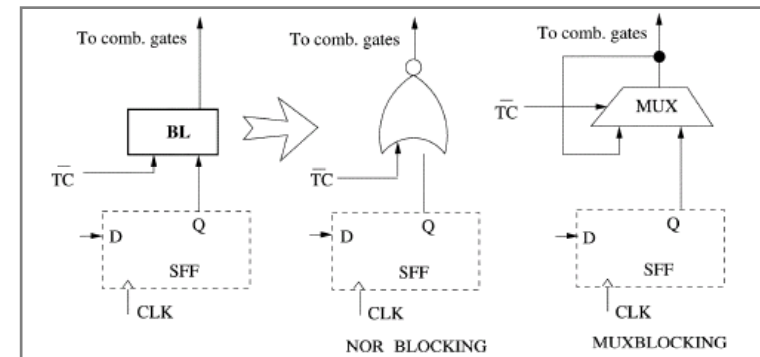
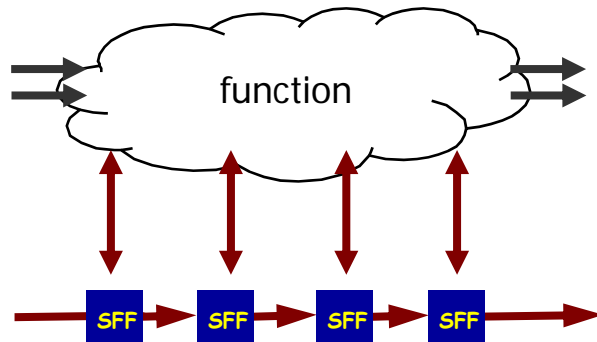


Gate Blocking

■ Power Reduction during Shift Mode

- FF Output Signal Disable
- FF with Low Activity

■ Drawbacks

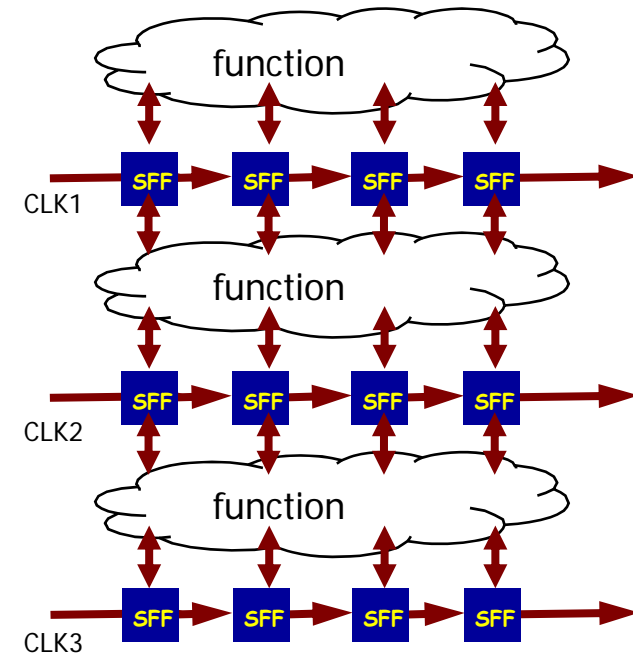
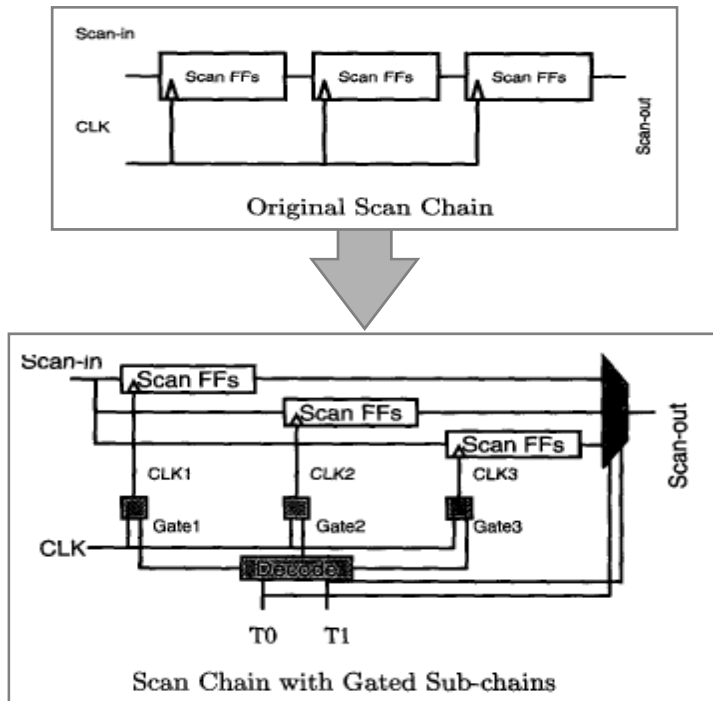


Design Partitioning

■ Design Partition with Clock Gating

- How to partition the device?
 - ◆ Test Time
 - ◆ Fault Coverage

■ Drawbacks



Design Partitioning

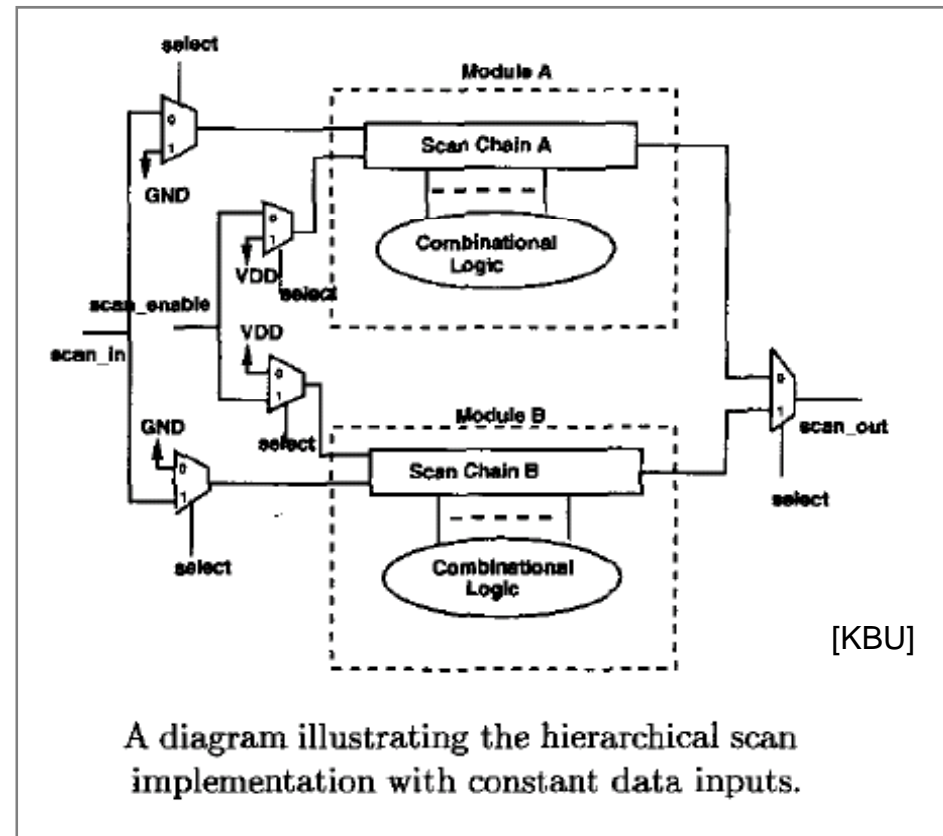
■ Design Partition with Multiple Scan Enable Signals

- How to partition the device?

- ◆ Test Time

- ◆ Fault Coverage

■ Drawbacks

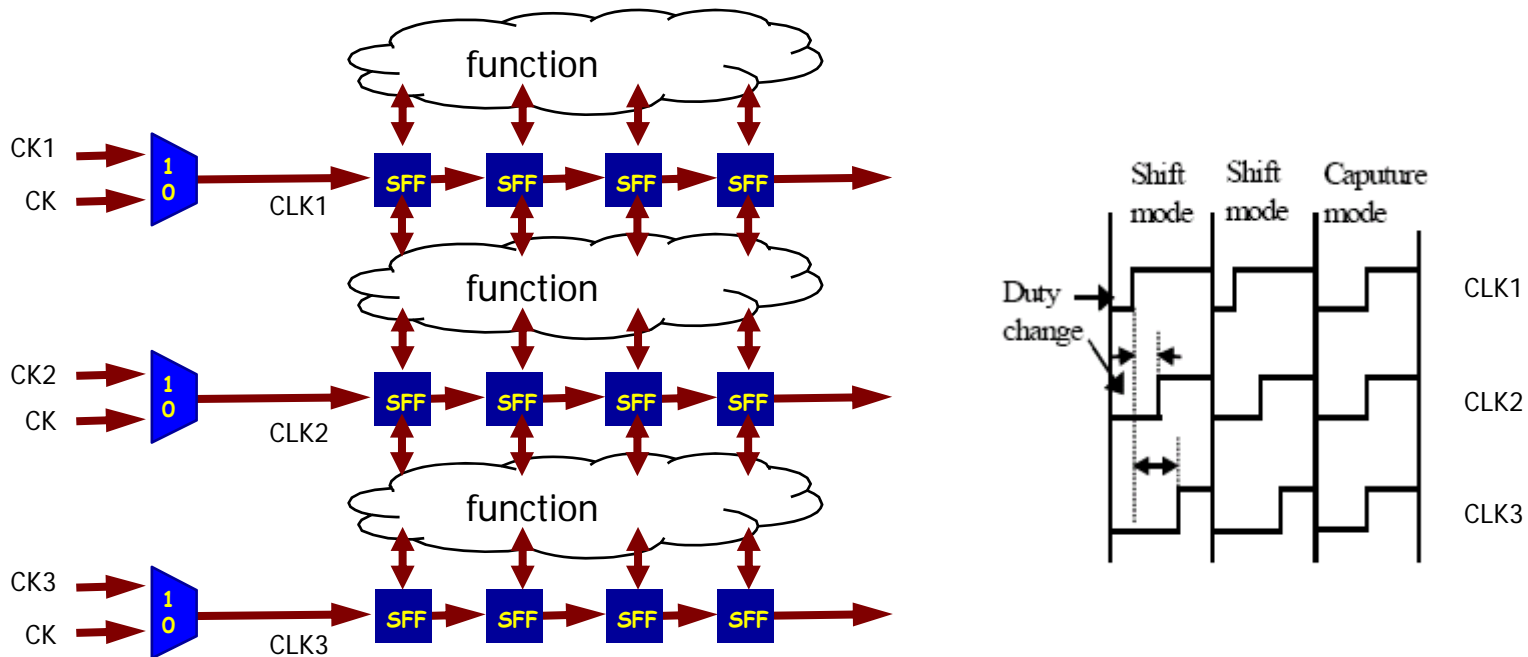


Design Partitioning

■ MD-SCAN (multi-duty scan)

- How to decide the duty depth?
- Different clock for shift and capture mode

■ Drawbacks



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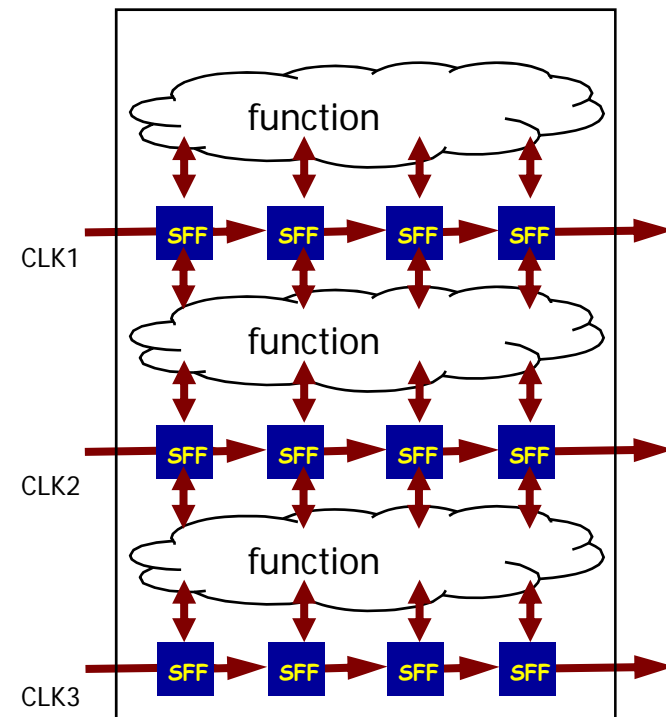
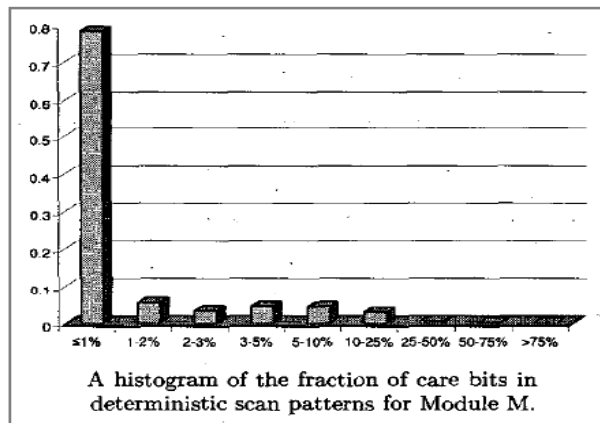
Test Pattern Modification

■ Random X-Filling

- Dynamic compaction for detecting more faults

■ Non-Random X-Filling

- 0-Filling
- 1-Filling
- Adjacent X- Filling



X	1	X	X	X	0	X	X	X	X	X	1
---	---	---	---	---	---	---	---	---	---	---	---

Test Pattern Modification

■ LCP (Capture Power Reduction) X-Filling

● Issues

- ◆ Target Selection Problem
- ◆ Value Selection Problem

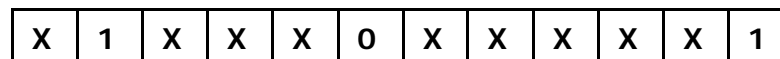
● Methods

- ◆ 0-Filling, 1-Filling, Minimum-Transition-Filling

➤ w/o considering the Impact of Capture Power

- ◆ X-Filling for Reduction of Logic Transition Count at Scan FF outputs.

➤ No Correlation with total Capture Power and Scan FF Transition



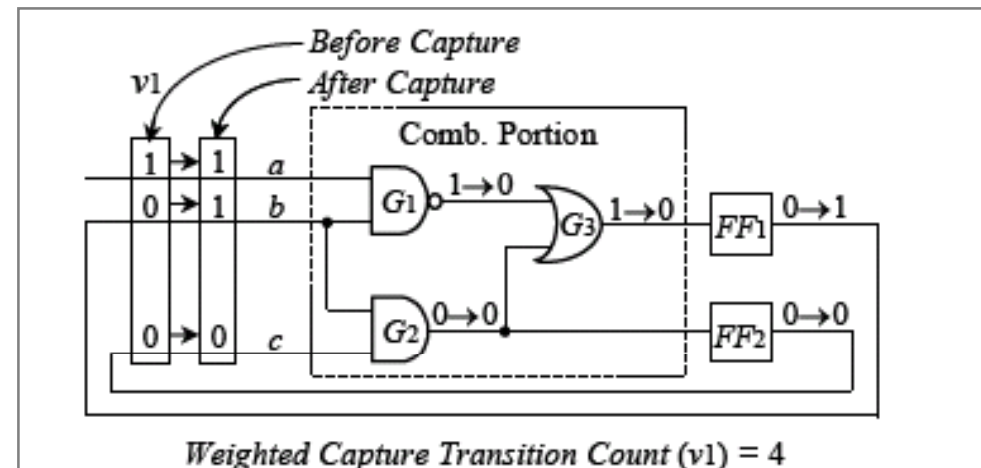
(1) target selection

(2) value selection (0/1)

LCP X-Filling

■ LCP X-Filling

- X-Score for *X-Filling Target Selection*
- Probabilistic Weighted Capture Transition Count for *X-Filling Value Selection*
 - ◆ The probabilistically-estimated number of weighted capture transitions at all nodes (gates and FFs)
 - ◆ Weight:
 - Toggles
 - Fan-out cone size

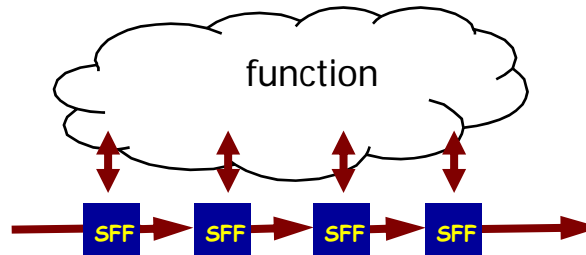


weighted capture transition count: (G1, G3, ff1)

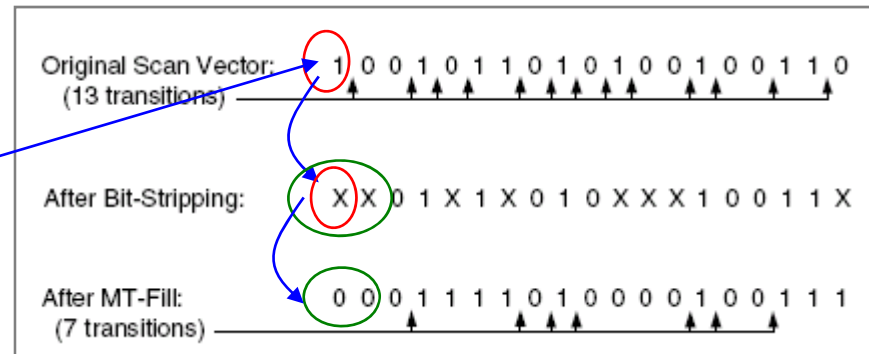
$$WCT(v1) = 1*1 + 1*1 + 1*2 = 4$$

Test Pattern Modification

■ Test Pattern Modification with Bit-Stripping



0이나 1로 검출되는
불량이 서로 동일함.

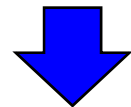


Test Pattern Compression

- Static Compaction considering Power Dissipation
 - Constraint WSA (Weighted Switching Activities)

V1 = X 0 X 0 X 0 X

V2 = 1 X 1 X 1 X 1

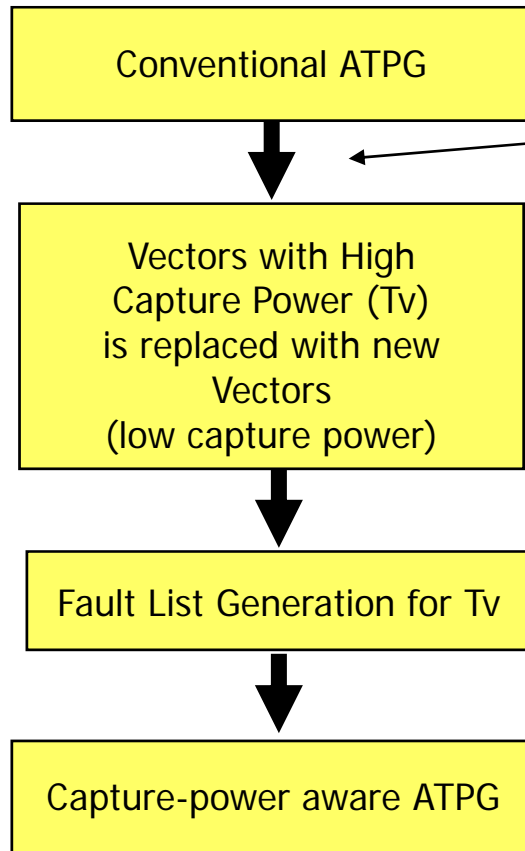


(6 Transition)

V0 = 1 0 1 0 1 0 1

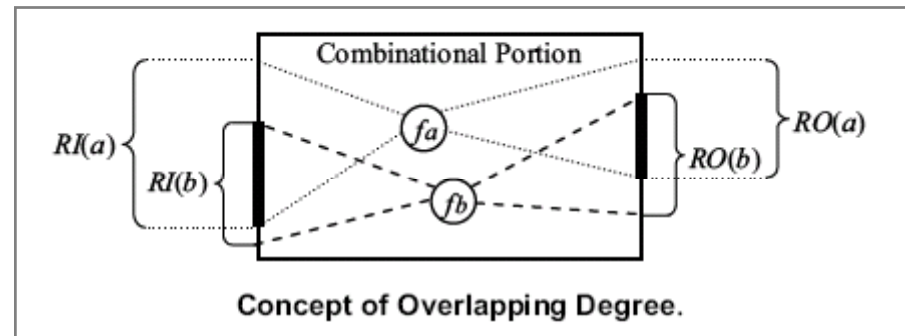
Power-aware ATPG

■ Low Power for Capture Mode



WSA

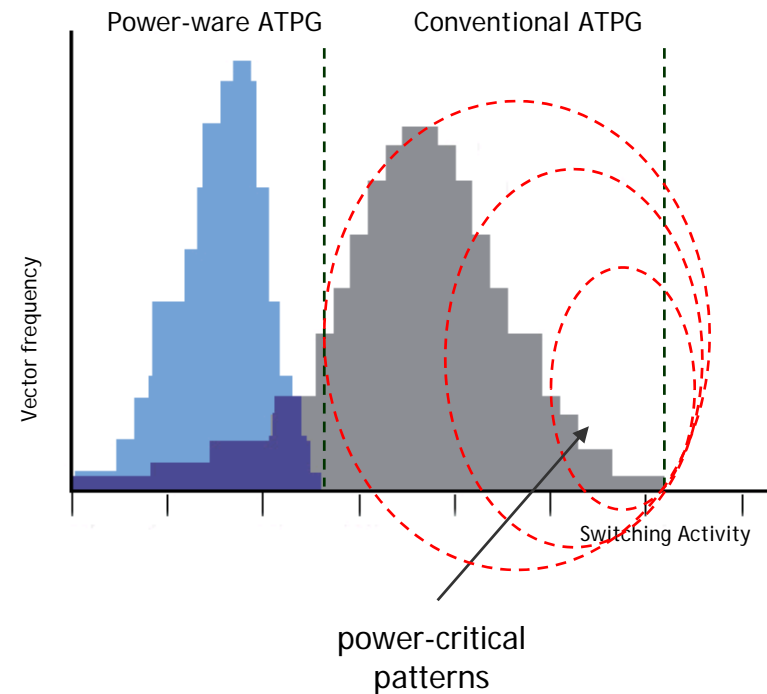
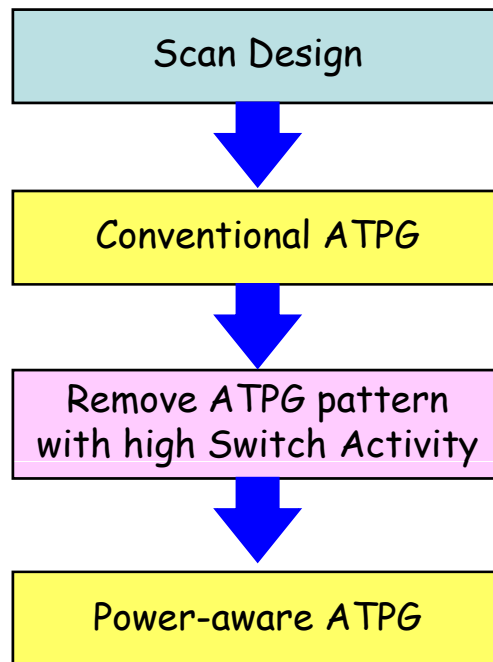
Max. allowed Threshold



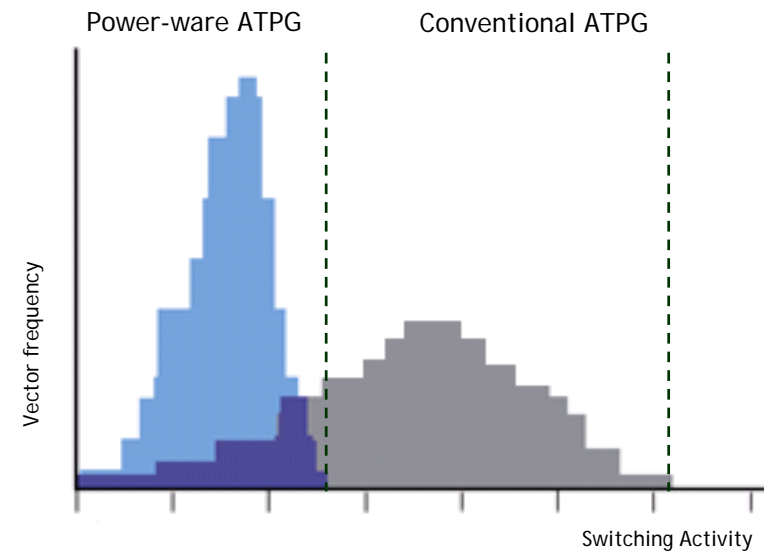
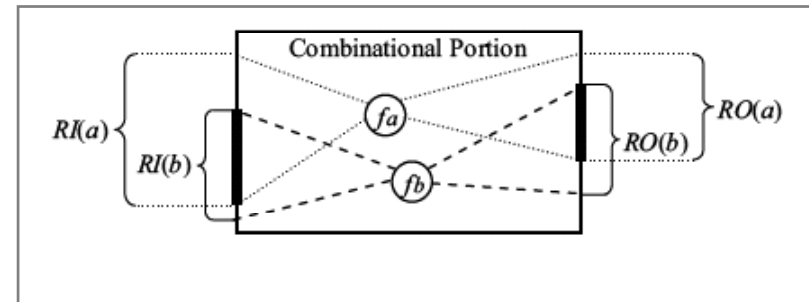
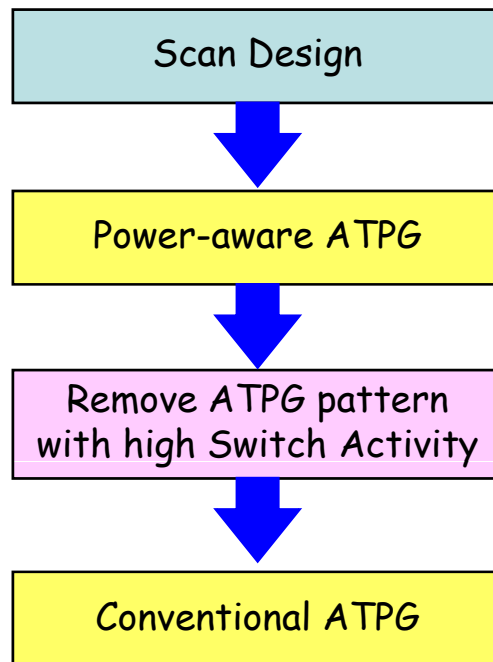
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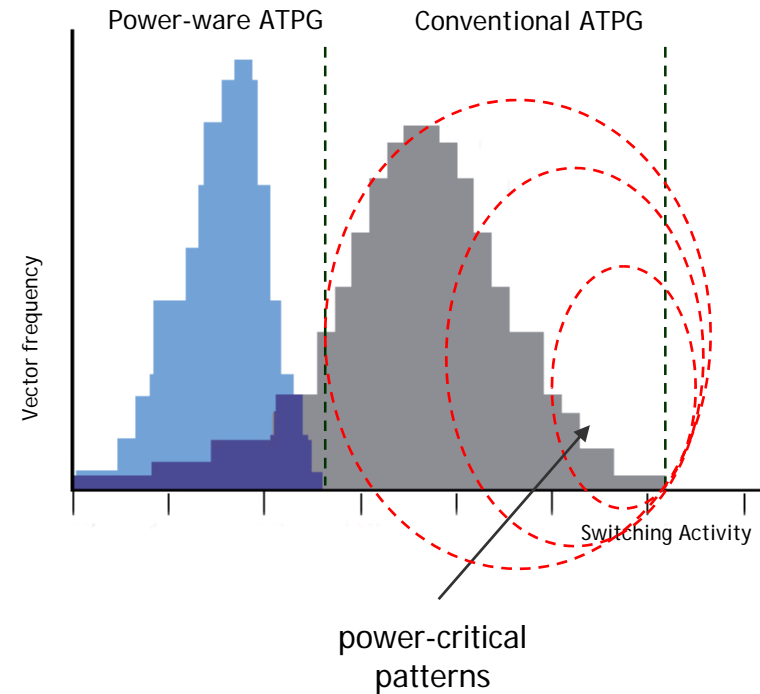
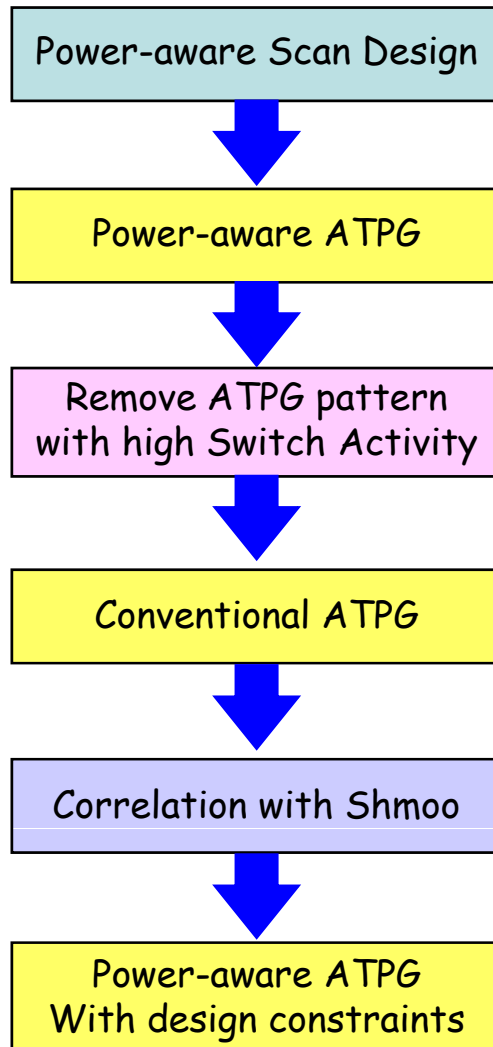
Power-Aware Scan Design & ATPG Flow



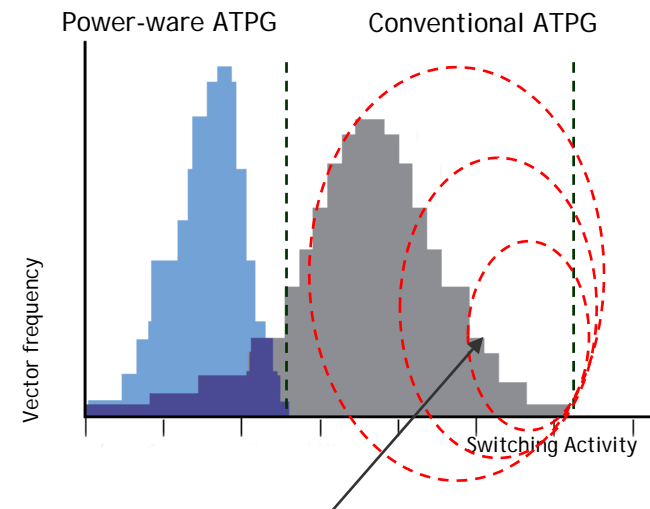
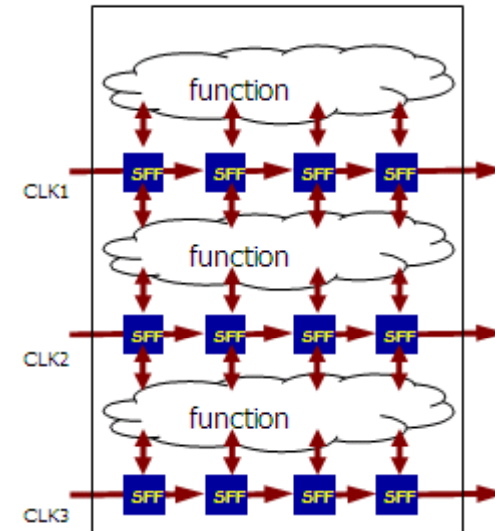
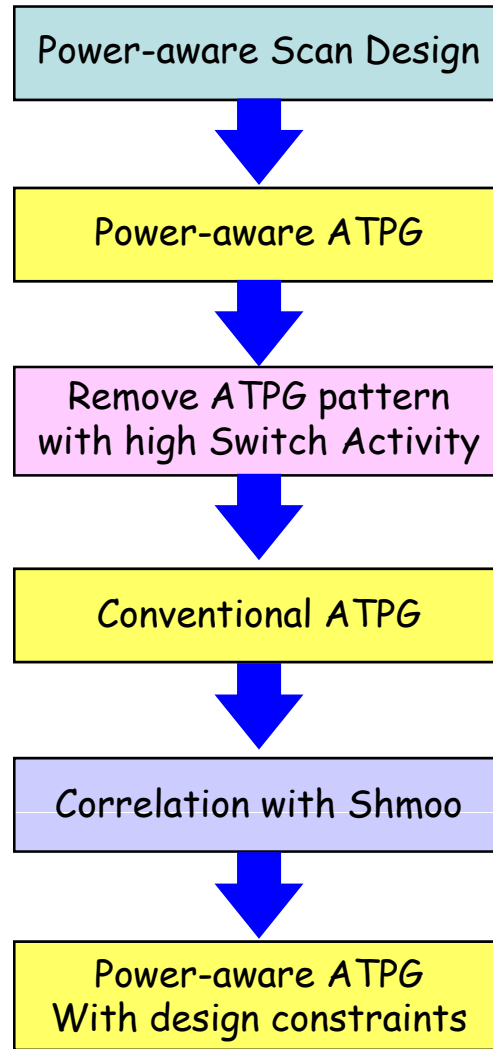
Power-Aware Scan Design & ATPG Flow



Power-Aware Scan Design & ATPG Flow



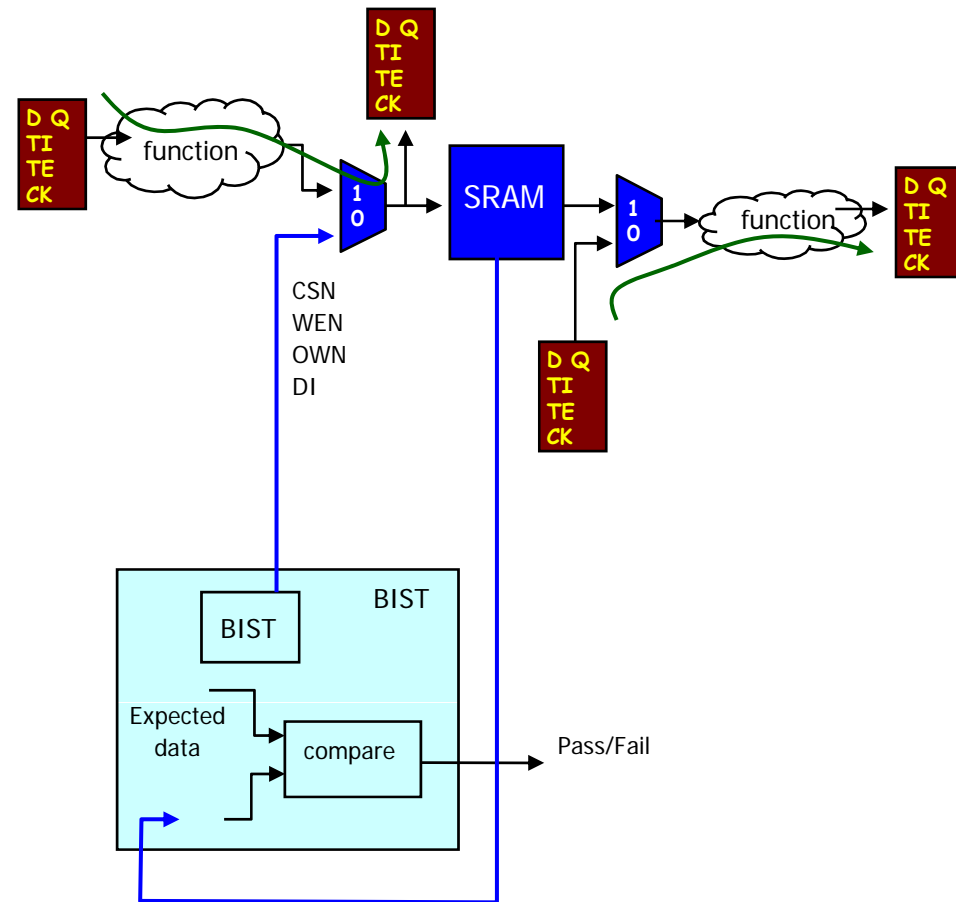
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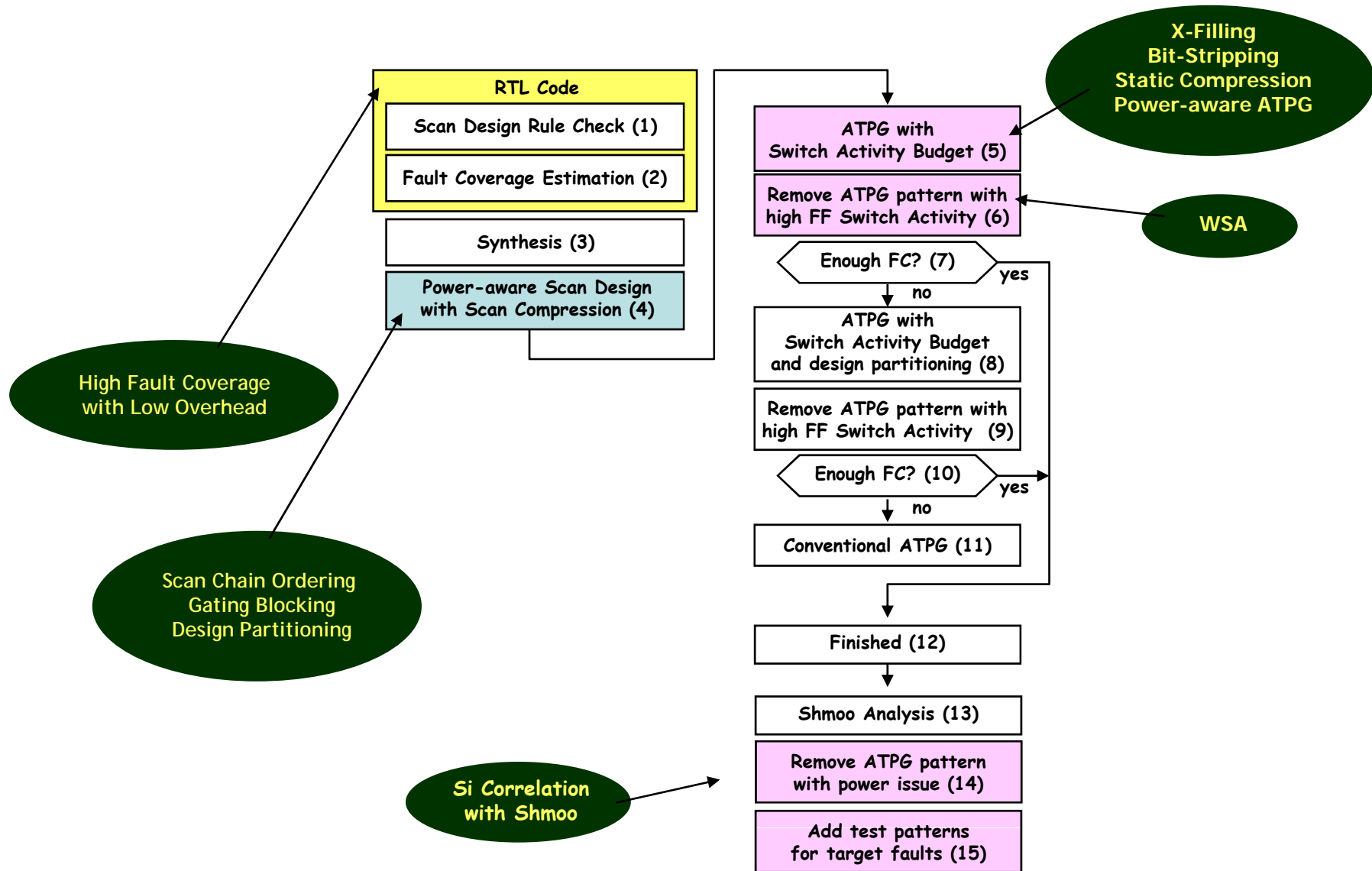
ATPG & Power Issues with Memories

■ Power issue of memories for ATPG

- ATPG w/ memories
 - ◆ Algorithm
 - ◆ Test time
 - ◆ Fault coverage
 - ◆ test quality
- ATPG w/o memories
 - ◆ memories: black box
 - ◆ memories are disabled



Example of Power-Aware Scan Design & ATPG Flow



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References

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