INNOVATION PUT TO THE TEST

FormFactor®
Advanced Wafer Probe Solutions

TSV Test

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Agenda

- TSV Test Issues
- Reliability and Burn-in
- High Frequency Test at Probe (HFTAP)
- TSV Probing Issues
- DFT Opportunities

TSV Device Testing

"Tools and methodologies for 3D IC testing regarded as the 'No.1 Challenge' among all EDA challenges for 3D IC design."

Ted Vucurevich, former CTO of Cadence Design Systems
at keynote speech at the 2007 '3D Architecture Conference'

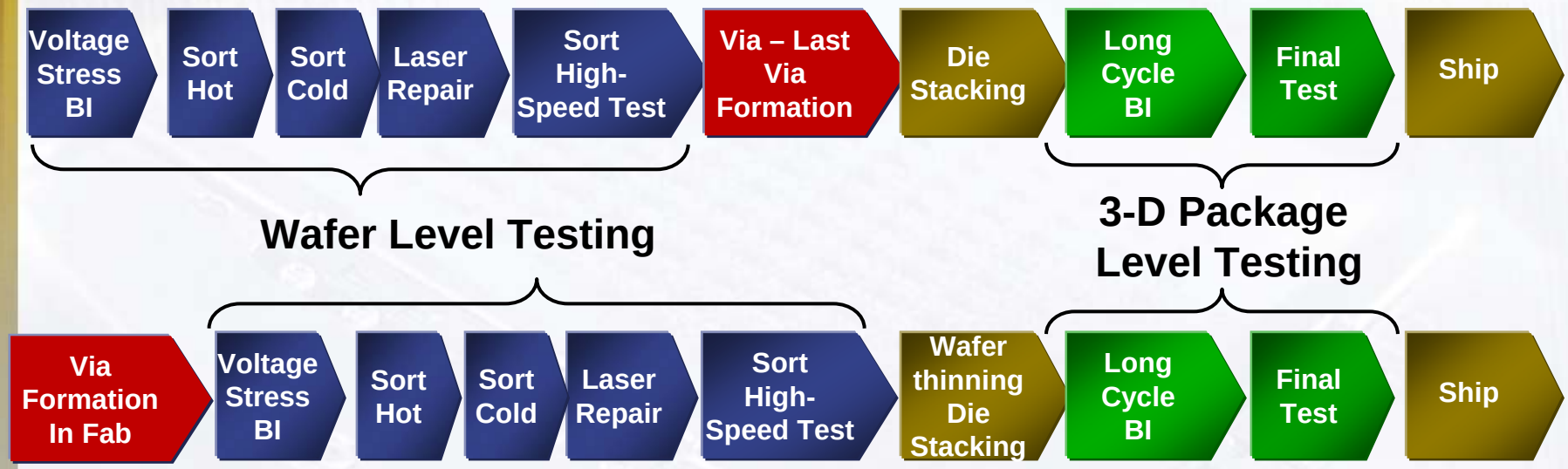
- TSV Device Test Objectives
  - Tests for new die defects
  - TSV interconnect test
  - KGD testing
- Challenges
  - 3D Test Flows
  - 3D Wafer Test Access
  - 3D DFT Architecture

TSV Device Test Objectives

- Tests for new die defects
  - Wafers thinned to 25-50 microns introduces stresses on memory structure
  - Temperatures > 250C in the via formation affect memory structure
- TSV interconnect testing
  - TSV formation yield not well characterized
    - Via-last could be as high as 1500 ppm – 15% 4 die stack yield with 300 TSVs
  - Die to die alignment
- KGD testing
  - Reliability testing – Long duration package like Burn-in at Wafer
  - Full specification test – at speed and parametric

TSV Test Issues

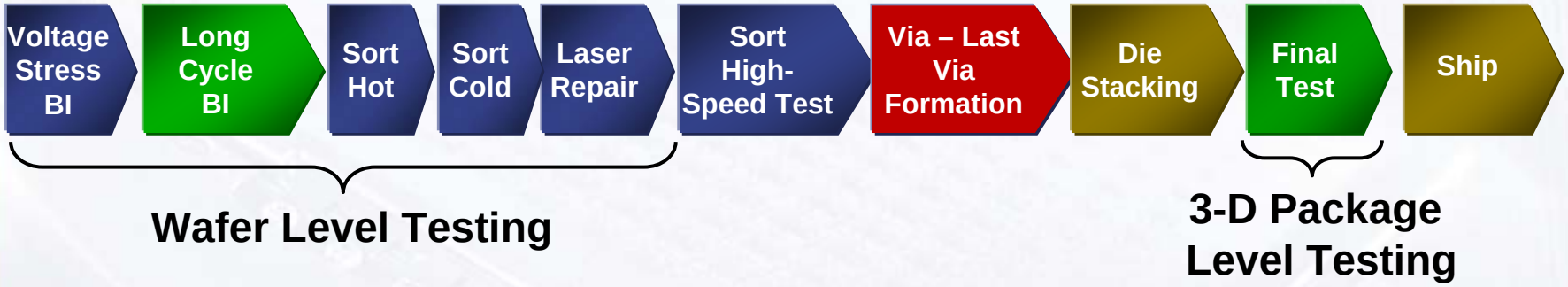
Today's most common DRAM TSV device test flow



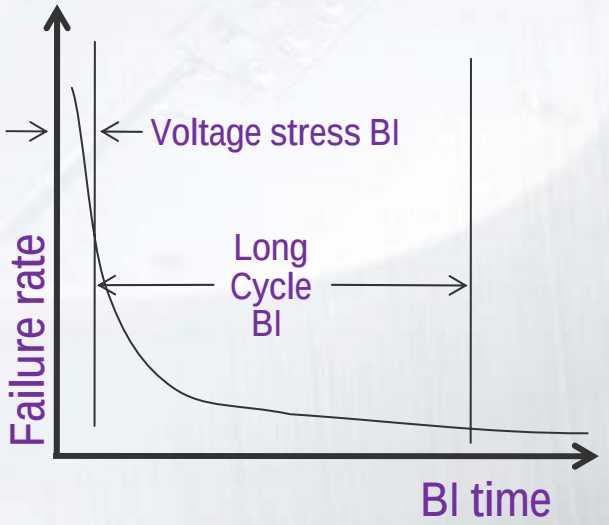
- Wafer level testing poses no new issues in this flow
  - Al pads
  - >50um pad size
  - > 60um pitch
  - Probing from top side of wafer

Wafer Level BI for TSV KGD devices

KGD optimization for DRAM TSV device test flow



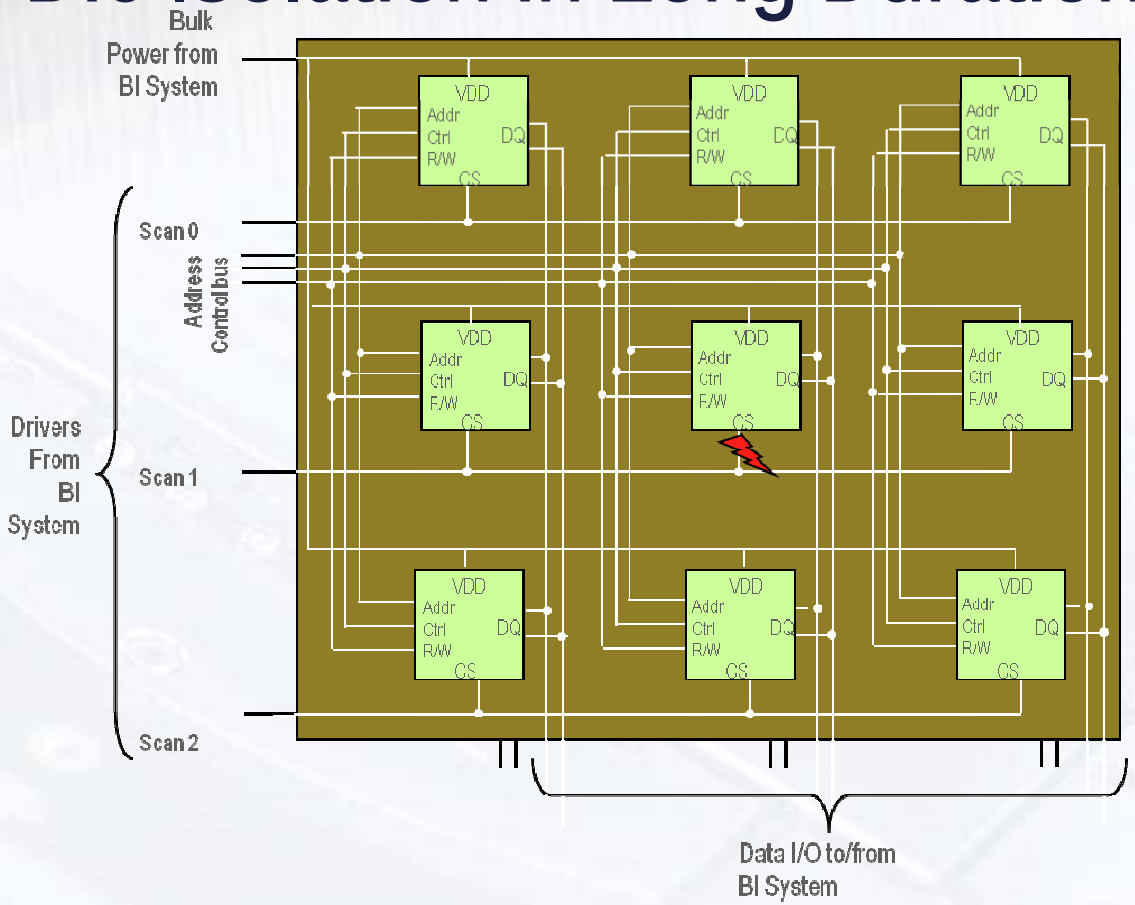
- Wafer level Burn-in
  - Voltage Stress BI
    - Causes some % of weak cells to fail
    - May be sufficient for some applications
  - Long duration BI (2-8 hours) before Sort steps in flow
    - Dynamic operating stress + Test



Pre-sort Long Duration Wafer Level BI

- Challenges to pre-sort long duration Wafer level BI
  - One Touch down required for cost effective BI
    - High contact count probe cards
  - Dual temperature may be required
    - Dynamic Operating Stress done at high temperature (125-150C)
    - Test done at a lower temperature (90-100C)
  - Isolation of bad devices from test matrix
- Advantages
  - Yield recovery though the normal sort / repair flow
  - Improved stacked device yield
- DRAM Device requirements
  - Low pad count for BI
  - Low signal count to permit very high parallelism on TDBI testers

Bad Die Isolation in Long Duration BI



- Use same approach as package BI with Scanning chip select
- 1 bad device can cause many device to not be Burned in
- Need to isolate bad devices from the test matrix

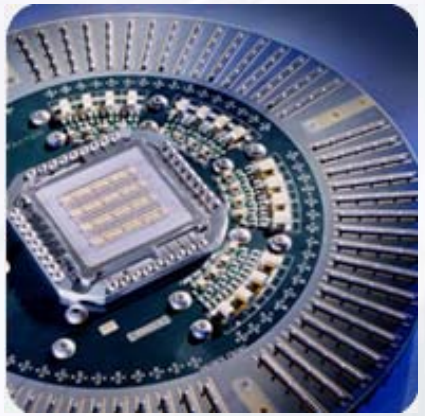
WLBI Solutions

- FormFactor Upstream WLBI
  - 1TD DRAM has been delivered
- Advanced Tester Resource Extension (A-TRE)
  - Expands parallelism of low parallelism testers up to 1 TD for BI
- Test temperatures up to 150C

Photo of 1 TD DRAM WLBI card

High Frequency Test at Probe HFTAP

- Challenge
  - Qualify and bin device to at speed performance
  - Limitation of tester parallelism
  - Limitation of high speed wafer sort testers – limit is 500MHz today
  - Test of TSV I/O structure at speed performance

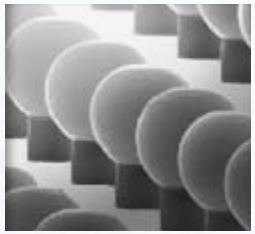


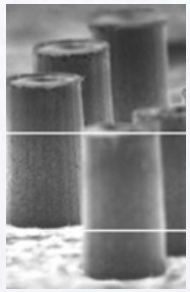
- Requirements
  - Clock rates to 500MHz
  - Data rates to 1000Mb/s
  - Low noise power distribution
- Solutions
  - FormFactor HFTAP K3 (300MHz / 600Mb/s) and K5 (500MHz / 1000Mb/s)

Challenges / Advantages of on TSV probing

Challenges

- TSV size and pitch
  - Via last
    - 20-30 um diameter, 40-50 um pitch
    - Cu-Sn micro balls
  - Via first / middle
    - 5-10 um diameter, 10-20 um pitch
    - Cu-Cu bonding



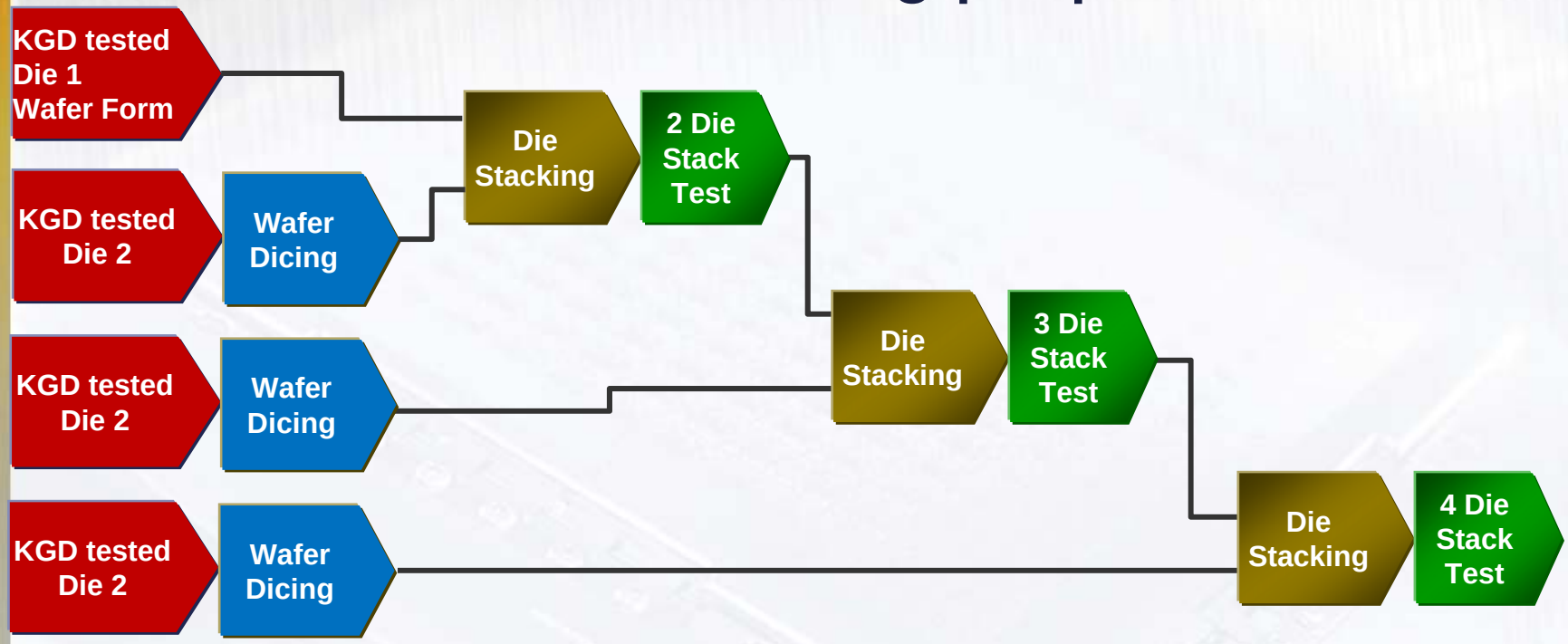


- Large number of TSVs (100s to 1000s)
  - JEDEC Mobile Wide I/O proposal ~1000 Vias / die
- Small or no ESD structures
- Can direct probing introduce staking yield loss
- Thin wafer (25-50um thickness on carrier wafer) probing

Advantages

- Improved stack yield, by detecting bad TSVs and TSV formation defects

Known Good Stack Testing proposal from IMEC



- Requirement
  - DFT for in process stack testing
  - Extra test insertions B
  - Back side test pads for stack testing
- Advantage – KGD devices for Die 3 and Die 4 are not put on known bad stacks
- Cost modeling needed to determine benefit

TSV Device KGD DFT Opportunities

On chip design for test circuits can aid in improving quality and lowering cost

- Reliability testing (Wafer Level BI)
  - Reduced pin count BI interfaces
  - On chip BI pattern generators – DOS time compression
- At speed test
  - Leverage technology from SoC at speed DFT for logic and I/O testing
- TSV integrity testing
  - Back side test pads
  - Redundancy for TSVs
- What are the alternatives to traditional KGD (e.g. fault tolerance)
  - Post stacking fuse repair
  - Overdesign for at speed performance
  - System level error tolerance

Thank You

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