SOC Device Trends

Mobile Smart phone, Tablet PC feature and devices
- more internet connection and cloud computing
- needs complex RF, Digital, PMIC chips

Easy to use by adding more human interface H/W and S/W
- Wide range of new devices with Sensors
SOC Device Design Trends and Architecture

Chaotic process of IC Design:
IP-based SoC designs have introduced new levels of complexity to the IC development process
- a multitude of design data from a variety of sources
- constantly changing design, requirements and process

Device Architecture Trends:
• Re-use of complex and 3rd party IP
• Asynchronous core interfaces
• Independent PLLs within IP cores
Complex SoC Device Feature & Test Demand

Demand for increasing test capability
- More data bandwidth ➔ 3G, LTE and LTE Advanced
- High speed interfaces ➔ Digital data rates
- Longer Battery Life ➔ Power management
- “More” connected ➔ More radio interfaces (GPS, WiFi, Bluetooth, FM, NFC)

Continuous cost reduction ➔ Higher throughput
Complex SOC Device Trends and Test

Advanced Packaging (TSV, WL-BGA)
Single Insertion Test
KGD quality requirements

Critical device quality requirements
More extensive testing
End-to-End functional test - “RF to bits”
Many RF and digital interface standards

Short product lifetimes
Rapid production ramps
Shorten test development cycles

Large volumes, Significant cost pressures
Increasing Multi-Site counts
Innovations for increase throughput

System in Package:
Source: Aspen Technologies
Continuous COT reduction for Customers

- Increased **throughput**:
  - Increased site count with higher density instruments & MUX modules
  - Improved single site test time & **parallel test efficiency** with features

- Increased throughput and yield with **New test strategies**:
  - Concurrent Test for reduced test times
  - Protocol Aware for reduced test time and retest

**Improve Customer’s Time to Market**

- Improve program development & debug time:
  - Test IP reuse & collaborative development
  - Concurrent Test development model and tools
  - Evolve from pattern to transaction programming with Protocol Aware

- IG-XL API’s to **interface the tester with design & production environments**
Multi-site capability is the key strategy to achieve low cost of test in SoC business

- 4-site codec in 2001
- 8-site CDP/DVDP in 2004
- 16-site Mobile A/V processor in 2007
- 32-site Mobile A/V processor in 2009
- 16-site Mobile A/V processor in 2011 and after
## More High Density Wide-Bandwidth Options for Reduction in COT

### Increased Performance for future devices

<table>
<thead>
<tr>
<th>Current</th>
<th>Compatible Transitions</th>
<th>2010 → 2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB6G: 8 Lanes</td>
<td>UltraSerial10G: 20 Lanes</td>
<td>10Gbps Serial (PA)</td>
</tr>
<tr>
<td>HSD1000: 64 Ch</td>
<td>UltraPin4000: 80/40 Ch</td>
<td>4Gbps</td>
</tr>
<tr>
<td>UltraPin800: 128 Ch</td>
<td>UltraPin1600: 256 Ch</td>
<td>1.6Gbps (PA)</td>
</tr>
</tbody>
</table>

### Digital Option

<table>
<thead>
<tr>
<th>BBAC: 2 Src / 2 Meas, 15MHz</th>
<th>UltraPAC80: 8 Src / 8 Meas, 80MHz+</th>
</tr>
</thead>
<tbody>
<tr>
<td>TurboAC: 2 Src / 2 Meas, 15MHz+</td>
<td></td>
</tr>
<tr>
<td>VHFAC: 2 Src / 2 Meas, 100MHz+</td>
<td></td>
</tr>
</tbody>
</table>

### AC Option

<table>
<thead>
<tr>
<th>DC30: 20 Ch</th>
<th>30V / 200mA</th>
<th>UltraVI80: 80 Ch, 7V / 1A (4A merged)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC75: 4 Ch</td>
<td>75V / 2A</td>
<td></td>
</tr>
</tbody>
</table>

### DC Option

- Increased throughput for higher site count with increased channel density

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**2001 Test Technology Workshop**

**November 16, 2011**

**James J. Ko**
Multi-Site Test and Parallel Test Efficiency

- **DIB (Mother) board**
  - High speed Digital and precision AC connections
  - Move AC applications to test head

- **Daughter board**
  - DC test application circuit and relays
  - 1 DC Block supports 4 sites testing
  - 8 copies of the DC Block for 32 sites

- **AC Expansion board**
  - Provide Common AC applications on test head for the multi-site AC testing

- **Option assignment**
  - North16 & South16 sites identical
    DIB design for testing independently

- **Symmetrical site to site circuit design**
  - Improve the site to site correlation
Vision for Concurrent Test

Two Flows, One Program

Serial Test Flow

Setup
Tests Core A
Tests Core B
Tests Core C
Tests Core D
Tests Core E
Tests Core F
Full Functional Test

Test Time

Concurrent Test Flow

Setup
Tests Core A
Tests Core B
Tests Core C
Tests Core D
Tests Core E
Full Functional Test

Concurrent Test Vision

Simple creation of a Concurrent test flow contained in the Serial test program

No changes to the tests code for serial flow or concurrent flow

Support Multiple levels of concurrency with distributed instrument control including Sync-Link (PSets/Signals)

Full support for Multi-site test and optimal Parallel Test Efficiency

Priorities:

#1) Minimize Development Time
#2) Optimize Concurrent Test Efficiency
Concurrent Test Program Development Process

Step #0 Planning
- Concurrent Core Operation
- DIB Design Checklist
- Resources Required per Core (DUT & Tester)

Step #1 Collaborative Development
- System Configuration
- Resource Conflict Checker
- Blocks can Operate Concurrently

Test Program Resource “Conductor”
- Function_Names
- Variable_Names
- DIB Design
- Concurrent Flow
- Common Pin Management
- Etc.

Step #2 Serial Test Flow
- Initial
- Tests Core A
- Tests Core B
- Tests Core C
- Tests Core D
- Tests Core E
- Tests Core F

Step #3 Concurrent Test Flow
- Initial
- Tests Core A
- Tests Core B
- Tests Core C
- Tests Core D
- Tests Core E
- Tests Core F
- Full Functional Test

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Software Environment: CTExec Software

Serial Test Flow

Concurrent Test Flow

Development Challenges

- Common bus/pins
- Shared test resources
- Flow manipulation
- Multi-site implementation
- Adaptive test & Retest
- Debug tools

Same Test code for **Serial** and **Concurrent** Flows
Software Environment: TimeLines Viewer

Development Challenges
• Common bus/pins
• Shared test resources
• Flow manipulation
• Multi-site implementation
• Adaptive test & Retest
• Debug tools
What is Protocol Aware Test?

**Protocol Synchronization & Communication**

**Protocol Level ATE**
- USB Signal Analyzer
- DRAM Emulator
- JTAG Analyzer

**Integrated Mobile Device**
- CPU
- DSP
- BB Proc
- JTAG I/F
- Mem I/F

**Protocol Level ATE Resources**
- DC Test Resources
- AC Test Resources

**Stored Response ATE**
- Execute fixed pass/fail vectors
- Slave DUT to tester
- Convert Design Information to Tester Language

**Protocol Level ATE**
- Interact with DUT using standard protocols (PCI-E, I2C, USB, LTE Advanced, etc)
- Adapt tester to DUT
- Use RTL level commands directly on tester

Modulated RF data generation/analyzer
3G
WiFi
First Generation Protocol Aware ATE

- Limited Protocol Aware ATE capability is available today
- A first generation Protocol Aware Instrument is the UltraFLEX SB6G
  - Designed for at-speed test of High Speed Serial buses like PCI Express and SATA
  - SB6G can recognize, manipulate, and compare 8b/10b encoded DUT output data

SB6G Timing and Data Alignment

DUT Output Data
- 6.4Gb/s Data Rate
- DUT output: 8b/10b encoded data @ up to 6.4Gbps
- Time align to incoming data
- Data align to specific 8b/10b Symbol Boundary
- Data manipulation:
  - Ignore Idles
  - Map +/- disparity
  - Re-map symbols
- Data align to a specific two symbol sequence

- At-speed compare with stored pattern
- At-speed compare with PRBS pattern
- Capture for later compare with Out-of-Order data

Capture for Out-of Order Data Compare
- Compare PRBS Auto-seed
- Compare Vector Data
Protocol Level ATE Architecture

- PA Architecture is Integrated into Standard Digital Functionality
  - PA or Standard Digital Programmable on a Pin by Pin basis
- Protocol implementation with FPGAs in datapath to minimize latency and support field upgrades
- Architecture supports configurable protocols to enable users to customize interfaces
- Architecture will support dedicated protocols to enable use of 3rd party IP
- FPGA Architecture Allows Flexibility
  - Upgrades Done in Field with Firmware/Software
  - Roadmap Updates Over Time

Diagram:
- Host Computer
- Logic Patgen
- DSSC
- FPGA Based Protocol Engines
- Timing
- Transaction Memory
- Select between normal PE operation and Protocol Aware
- Pin Electronics
- PE
- DUT
Direct Read and Write of Device Registers

**Strategy with Stored Response ATE**
- Translate JTAG commands into multiple parallel vectors
- Develop software wrapper to dynamically generate patterns and decode results

**Strategy with Protocol Aware ATE**
- Patternless commands to read and write registers in native protocol

**Potential benefits**
- Faster program development
- Faster test time
- Up to 98% smaller pattern sets

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Write.jtag (ADDR:04h, DATA: 55h)
Read.jtag (ADDR:0Ah, DATA → read_var)
Cost of Test Reduction

Increasing site count for lowest COT

DIB/Probe Card
Mother/Daughter Board

Z-space DIB Modules

Test head Enablers

Instrument Pin Density

Device Specific

Device Family

Market Segment

Universal Instrument

DIB/Probe Card
Mother/Daughter Board

Z-space DIB Modules

Test head Enablers

Instrument Pin Density

Increasing site count for lowest COT
DIB Modules for multi-site DAC Testing

DC reference Module
FLEXConnect: Market Segment Enabler

Improving Test Development time and increasing high-site count DIB reliability

By reducing applications circuitry on the DIB

Existing Modules include
DC Enabler – (32) 1A Relays
High Current Switch Matrix – (4) 1:6 MUX’s
Towerless Probe for TSV and Bumped die

Advantages:
- Higher signal fidelity
- Lower tooling costs
- Better planarity with chuck
Design → Test → Design Loop

**Failure Analysis / Yield Enhancement**

- On-Tester Debug/Characterization (hours/minutes)
  - Timing/Levels
  - Mixed Signal
  - Repeatability
  - Correlation

- **“off tester” tools**
- **“on tester” tools**

**EDA-based Pattern Viewer**
- Simultaneous display of EDA and tester information
- Diagnose Physical Device Faults

**Pattern & Test program. Gen.**

**ATPG**

**Design**

**Simulation**

**STDF**

**20011 Test Technology Workshop**

November 16, 2011

James J. Ko
Summary: SOC ATE System Design for TFx

Complex SoC design and test demand
- Use more Sensors, H/W and S/W for better human interface
- Low power, high speed for mobility
- Re-use of 3rd party IP
- Use Asynchronous interfaces IP cores
- Low cost of test and high production efficiency
- Easy program development and ATE optimization tools for Time to Market

ATE system design for the new SoC and test demands
- High BW RF, high speed Digital, accurate DC
- Protocol Aware for testing Asynchronous independent IP cores
- Test IP reuse & collaborative development tools
- Multi-site test and Concurrent test for low COT
- Precise wafer probe interface
- Link to EDA tools -Test to Design for Time to Market