The challenge for memory test
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The challenge for memory test

- **High speed test**
  - Mobile KGD test
  - Package high speed channel sharing

- **Fine pitch device test**
  - PCB Technical limit
  - Fine pitch socket

- **TCR (Test Cost Reduction)**
  - Probe 1-T/D Solution
  - Low Cost Tester
  - Legacy tester life cycle extension
High speed test (1/5)

1-1. Mobile KGD Test

Mobile Device Demand Growth for Various Entertainment Product

- Low Power, High Performance Memory
- Small foot print Product
- MCP, Embedded Product

→ High Speed KGD Test will be needed

KGD Test Challenges

- Over 500Mhz to 1Ghz probe test is possible
  
  Present System→ 280 ~ 400Mhz ..Too Slow !!!

- Probe Card is possible in speed. But Parallel is Too small !!!

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1-2. High Speed Probe CARD

- Low parallelism
- Crosstalk, noise minimize
- PCB size (space) limit
2-1. Package high speed channel sharing

- DDR4 Data rate 2.4~4.0Gbps
- Package test system speed Max 8Gbps
- Test Parallel & DR Channel Sharing?

<table>
<thead>
<tr>
<th>Parallel</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>512</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>1Gbps &lt;</td>
<td>1Gbps &lt;</td>
<td>1 ~ 2Gbps</td>
<td>2 ~ 4Gbps</td>
<td></td>
</tr>
<tr>
<td>Sharing</td>
<td>-</td>
<td>2</td>
<td>4</td>
<td>4 or 8</td>
<td>4 or 8</td>
</tr>
<tr>
<td>Method</td>
<td>T-Branch</td>
<td></td>
<td>Daisy-Chain</td>
<td></td>
<td>Daisy-Chain</td>
</tr>
<tr>
<td></td>
<td>Timing Error?</td>
<td>Tr / Tf?</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2-2. Signal integrity for sharing high speed channel

- Technical development needed for efficient TR/TF performance
2-3. Timing Error: RC time delay

- High frequency affects on timing error growth
- Test hardware limit
- Timing training solution needed to reduce Skew & Timing error

### Timing Error according to capacitance change

<table>
<thead>
<tr>
<th>DUT</th>
<th>C (pf)</th>
<th>Z (ohm)</th>
<th>tRF (ps)</th>
<th>tRF (BR)</th>
<th>tRF (RSS)</th>
<th>tRF ( fe )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>50</td>
<td>50</td>
<td>60</td>
<td>50</td>
<td>125</td>
<td>63</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>10</td>
<td>60</td>
<td>125</td>
<td>100</td>
<td>83</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>10</td>
<td>50</td>
<td>200</td>
<td>100</td>
<td>37</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>50</td>
<td>50</td>
<td>220</td>
<td>144</td>
<td>51</td>
</tr>
</tbody>
</table>

- Rise time of driver: $\tau_{RF} = 60 \text{ ps}$
- Rise time of RC filter: $\tau_{RF} = 2.2 \times RC$
- Rise time at DUT: $\tau_{RF} = \sqrt{\tau_{RF1}^2 + \tau_{RF2}^2}$

Channel Skew
1-1. Fine pitch device test

**Fine pitch device test challenges**

- Ball pitch 0.8 >> 0.5 >> 0.4 >> 0.35
- PCB limit & Yield Down
- Expensive Interface Cost (socket price increased)
  - PCR 0.4pitch : X, POGO 0.3pitch : OK but expensive
- Contact Faulty (open, short, leakage fail, low yield, ball damage, retest...)

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**Main Memory**

- **0.8 pitch**
- **0.5 pitch**
- **0.4 pitch**
- **0.35 pitch**

**Mobile (PoP)**

- **Contact pin count**

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**0.25mm**

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**0.4mm**

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**Chip**

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**Substrate**

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**Solder Ball Height**

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**Ball Pitch**

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**Au Wire**
1-2. Fine pitch PCB Limitation

Drill process of fine pitch PCB causes yield drop
- 0.3 pitch, Drill Tolerance < 20um
- Current technology is impossible
  → New technology needed (Pitch Converter?)

<table>
<thead>
<tr>
<th>Pitch</th>
<th>-</th>
<th>0.5mm</th>
<th>0.4mm</th>
<th>0.3mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drill</td>
<td>A</td>
<td>0.25mm</td>
<td>0.15mm</td>
<td>0.15mm</td>
</tr>
<tr>
<td>Drill to Pattern</td>
<td>B</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.05mm</td>
</tr>
<tr>
<td>Inner Layer Pattern</td>
<td>C</td>
<td>0.05mm</td>
<td>0.05mm</td>
<td>0.05mm</td>
</tr>
<tr>
<td>Drill Spec</td>
<td></td>
<td>0.15mm, Tolerance 0.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normal Tolerance</td>
<td>Drill+D/F+layer Up Tolerance</td>
<td>0.1mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Special Tolerance</td>
<td>Drill+D/F+layer Up Tolerance</td>
<td>0.020mm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
1-3. Fine pitch Socket

- **Contact accuracy**
  - Ball vs socket pin price goes down, on the other hand short fail increase
  - Managing device size tolerance needed
  - Thin diameter causes socket pin damage

- **Solution**
  - Floating guide (Direct contact) : 0.3 pitch PCB limit
  - Pitch convert technology is very complicated and weak on Si
  - Wireless (Inductive Coupling)
Test Cost Reduction (1/4)

- High density product demand increase with IT trend
- 1 Die FAB Cost down: Tech Shrink (refer to the left graph above)
- 1 Die TEST Cost up: Density / Net Die growth (refer to the right graph above)

TCR (Test Cost Reduction)

TTR, DFT, parallelism, low cost tester, reduction of test process, optimum batch size, selective test by grade, etc..
1-1. Probe test Parallelism Up

**How to increase the parallel on Probe?**

**Target could be**

**1Wafer 1TD Testing**

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<table>
<thead>
<tr>
<th>Probe Card</th>
<th>Tester</th>
</tr>
</thead>
<tbody>
<tr>
<td>• High signal sharing, Worst input margin</td>
<td>• Platform expansion, system cost up</td>
</tr>
<tr>
<td>• Smaller mount space, complex circuit design</td>
<td>• Partition architecture, more flexible DUT mode</td>
</tr>
<tr>
<td>• High probe count, Mechanical deflection</td>
<td>• Internal relay sharing</td>
</tr>
<tr>
<td></td>
<td>Poor S.I &amp; power dividing</td>
</tr>
</tbody>
</table>
1-2. PKT Low Cost Tester

ATE Limitation

- More IO Channel needed for Test
  - x4, 8, 16, 32 → x64, 512, 1024 ~

- Package test Parallel extension limit
  - IO Channel shortage
  - High test interface cost
    ( Handler, Interface Board, Socket )

- Channel sharing limit
  - x2 / x4 / x8 → x16 sharing?
  - Signal integrity weakness
  - Yield drop, dc test accuracy weakness

Low Cost Tester

- Product optimized function
- Low frequency for core test
- Low cost per 1 Channel
- FPGA use, Easy upgrade
1-3. Legacy tester Life cycle extension

**Package BOST System**

- **Current BOST system limitation**
  - DC test X (FPGA/ASIC use)
  - Cooling problem for BOST Chip heating
  - Constraint on test process

- **New BOST system needed**
  - DC test function on BOST
  - Water cooling system
SUMMARY

- **High Speed Interface Technology**
  - High Speed Probe CARD parallel extension
  - High Speed Channel Sharing Technology

- **Fine pitch device contact**
  - Contact problem according to pitch downsize
  - PCB, socket accuracy improvement and cost reduction

- **TCR (Test Cost Reduction)**
  - Probe 1-T/D test solution
  - Low cost tester
  - New BOST system for DC Test