DFT Challenges in 3D ICs

2012 Test Technology Workshop (Oct. 31, 2012)

Kun Young Chung
Design Technology Team
System LSI
Samsung Electronics
Contents

- An Overview: Test Challenges in 3D ICs
- Design (Design-for-Test) for 3D ICs
- Test for 3D ICs
- Yield for 3D ICs
- What should we do now?
- Future perspectives
Today’s Topic

• **What 3D-IC?**
  - Memory + Memory
  - Logic + Memory
  - Logic + Logic
  - Heterogeneous (Logic + Memory + RF + MEMS + Battery + ...)

• **Are you ready for volume production?**
An Overview: Test Challenges in 3D ICs
Test Challenges for 3D Integration


• **Wafer probing**
  • Major limitation for thinned wafers and pre-bond wafers

• **Known-good dies (KGD)**
  • KGD again? KGD w/ TSV
  • Testing needed to ensure structural integrity and performance of stacked modules

• **New failure mechanisms?**
  • Extra steps: Thinning, alignment, and stacking → changes of defects increase
  • During bonding, particle caught b/w wafers → peeling and delamination → drop bonding quality and yield
  • Edge effect must be considered: edges b/w bonded wafers are more susceptible to chipping, peeling, and delamination (unique problems in 3D ICs)
  • Cracking due to loading forces, backside grinding, and die thinning
  • Random open defects can result from dislocations, oxygen trapped on the surface, voids formation, and mechanical failures
Test Challenges for 3D Integration

• **Thermal and power-delivery considerations**
  - Test patterns must be generated to target hot regions on different layers and hot TSVs

• **SOC test access and test scheduling**
  - Much more complexity than in 2D: Embedded cores may be on different layers
  - TAM (Test Access Mechanism) optimization and test scheduling
    - Must consider thermal and power constraints
    - Capable of transporting test data to the cores, and transferring test data to dies from stack input/output pins
    - Capable of testing individual dies as well as testing of partial and complete stacks at low cost

(Source: Marinissen (IMEC), et al., VTS, 2010)
Test Challenges for 3D Integration

• Reliability and testing of TSVs post-bond
  • TSV yield will drop as # of TSVs increases (over tens of thousand?)
  • Even a single TSV defect in post-bond can void the entire chip stack, reducing the yield
  • Redundancy and self-repairing (especially for transmitting signals)
Test Challenges for 3D Integration

- **Wafer test ATE**
  - Should have very large vector memory depth
  - Capture memory should be almost equal to vector memory
    - Structural fail data can be very large
  - Power supplies should have high \( \frac{di}{dt} \)

- **Wireless test interface??**
  - Project HOY – National Tsing Hua University, Taiwan
    - Wireless interface for test – BIST based
    - To eliminate probe wires
    - Tester becomes a wireless receiver
Design (DFT) for 3D ICs

SAMSUNG ELECTRONICS
System LSI Business
**TAM (Test Access Mechanism)**

- **Must provide test access to all the test features on every die**
  - Similar to providing test access to chips on a board
  - Should have hierarchical access to test controllers

- **Key requirements**
  - Access internal test features of embedded silicon
  - Test interfaces b/w different stacked devices

- **Standardized**
  - IEEE 1149.1
  - **IEEE 1500**
  - IEEE 1149.7
  - **IEEE P1697** (iJTAG; instrumental JTAG)
  - **IEEE P1838**
TAM (Test Access Mechanism)

- **Test access architecture**
  - Structured and scalable TAM
    - Marinissen, et al. VTS2010
    - IEEE1149.1 & IEEE1500
  - Test integration methodology
    - Chou, et al. ATS2010
    - IEEE1149.1 & modified IEEE1149.1
  - Works presented using IEEE P1687
  - IEEE P1838
    - Test access architecture for 3-D stacked ICs
    - Upcoming: IEEE int’l workshop on 3D-TEST (Nov. 8-9 at ITC2012)
    - Leverage existing DFT
      - IEEE 1149.x
      - IEEE 1500
      - IEEE P1687

Good TAM for DFX (DFT, DFD, DFY, DFR, ...) will be the key!!
• **Test optimization for test cost minimization of 3-D ICs**
  - Scan chain construction for 3D ICs
    - Wu, et al. ICCD 2007
    - Average wire length reduced
    - But when will it become useful?

• **Test-wrapper optimization for embedded cores in 3D SOCs**
  - Noia, et al. ICCD 2009
  - Wrapper chain length reduction
  - Optimize = func(TAM width, # of TSVs)
  - What about pre-bond test? Micro probing?
Some Publications on Design Side

- **Layout-driven consideration**
  - **Thermal aware test scheduling for 3D SoCs**
    - Layout driven test architecture for core-based SoC
    - Pre-bond test-pin count constraint
    - Thermal aware test scheduling
    - To eliminate thermal hot spots during test

- **Layout-driven test-architecture for 3D SoCs**
  - Jiang, et al. ICCAD 2009
  - Pre-bond test-pin count constraint
  - Sharing of test wires b/w pre-bond & post-bond

![Test architecture for 3D SoC](source: Jiang, et al. TonVLSIS 2009)
Test for 3D ICs
Pre-bond Defects and Testing (Noia and Chakrabarty, ITC 2011)

• Pre-bond defects
  • Can impact chip functionality
  • Forms of defects
    - Incomplete metal filling or microvoids in TSV: increase resistance and path delay
    - Partial or complete breaks in TSV: resistive path or open path, respectively
    - Impurities in TSV: increase resistance and interconnect delay
    - Pinhole defects: leakage path to substrate
      \[ \Rightarrow \text{increase capacitance b/w TSV and substrate} \]

• Pre-bond testing
  • Need to detect TSV defects prior to bonding
  • Defects change TSV resistance and capacitance
  • Difficult due to TSV pitch and density (will shrink further)
    - Difficult or impossible for one probe needle to contact a TSV

(Source: Noia & Chakrabarty, 2011)
**Pre-bond Defects and Testing**

- **Pre-bond test**
- **DRAM-like test using sense amp.**
  - Chen, et al. ATS 2009 & VTS 2010
  - Capacitive and resistive modeling
  - Factors: discharge current and time, sense amp threshold
  - But transmission gates for TSVs in SOC?
  - Q: Calibration? Pass/fail criteria??

(Source: Noia & Chakrabarty ITC 2011)
Pre-bond Defects and Testing

- **Pre-bond probing**
- **Pre-bond probing of TSVs**
  - Noia & Chakrabarty ITC 2011
  - Measure resistance and capacitance
  - Stuck-at and leakage tests
  - One-to-many mapping
  - Proof of concept using HSPICE sim.
  - But practical? Resolution good enough?

(source: Noia and Chakrabarty, ITC2011)
• Pre-bond probing (cont’d)
  • Micro-bump probing for wide I/O testing
    - Smith, et al. ITC2011
    - Lithographic-based MEMS probe card
  • NanoPierce™ contactor for micro-bumps
    - Yaglioglu and Eldridge VTS2012

(Source: Smith, et al. ITC2011)

Figure 4: Flexible NanoPierce™ contactor with 1104 interconnects on 40μm x 50μm grid. Inset shows SEM image of the interconnects.
(Source: Yaglioglu and Eldridge VTS2012)

People wouldn’t let go of pre-bond probing?
Test quality good enough?
- Confident to throw away when faulty?
Pre-bond Defects and Testing

• Pre-bond self test
  • TSV defect/pinhole self test circuit
    - Tsai, et al. Int’l Conf. on 3D System Int. 2009
    - Analog self-test circuits proposed
    - Leakage current used to measure TSV-to-substrate resistance

Many works done in the context of “Let’s make it happen”

Now we really need cost-effective & reliable pre-bond test method
and optimized test flow
Post-bond Defects and Testing

• **Post-bond defects**
  - Oxidation or contamination of bond surface
  - Height variation of TSVs
  - Particle between two dies
  - Misalignment during bonding

• **Post-bond testing**
  - **Interconnect test**
    - For single ended CMOS I/Os
      - Traditional transition test
      - For very dense TSVs, some coupling effects
    - For differential I/Os like SERDES
      - I/O loopback or BIST need to be considered
      - Need to measure the “eye opening” to calculate effects of Jitter and Noise
    - TSVs that provide power supply
      - Need to be characterized for IR drop and di/dt characteristics
  - IO BIST?
  
• **Q: Really interconnect test needed? Yes**
Post-bond Defects and Testing

• **Post-bond testing**
  • **BIST of TSVs**
    - Arrange TSVs into arrays similar to memory
    - Low test and diagnosis time and low silicon area cost
    - But detectable defects may be limited

• **Q: Each chip was claimed to be a KGD. Do we need re-testing?**
Other Post-bond Issues

• Thermal and power issues
  • Power issues
    - IR drop and di/dt need to be monitored with power sensing and correction
    - Will need a network of power sensors that are accessible through a serial common interfaces (e.g., iJTAG)
  • Thermal issues
    - Will require thermal monitor on various sections of 3D stacks
    - Will require a network of temperature sensors accessed through a common serial interfaces (e.g., iJTAG)

**Test must consider power and thermal and should not overkill**

- Increased hot-spots due to increased power density
- Power connection through dies underneath:
  → Increased IR-Drop
Yield for 3D ICs

Focus on Redundancy and Repair
Redundancy and Repair

- **Redundancy and Repair**
  - Similarity with memory redundancy and repair
  - TSV repair for 3D stacked ICs (Jiang, et al. DATE 2012)

- **Issues/challenges**
  - Muxes affordable? Performance degradation?
  - Regular array or irregular array?
  - Isn’t your TSV yield high enough that redundancy doesn’t pay off?
  - Are you sure the TSV is the culprit? (Accuracy of diagnostics)
Redundancy and Repair

- As TSV density increases, TSV induced defects will increase
  - Redundancy and repair will be indispensable for yield
- Memory redundancy is very common for modern SOCs
  - Allows to yield devices even in the presence of high defect density
What should we do NOW?
• **TSV defect analysis**
  • Failure modeling, characterization
  • Failure detection
  • e.g., 2012 TSV Test and Technology Workshop (TERA, KAIST)

• **What’s lacking in and growing concerns**
  • Need a way to detect and diagnose open/short defect in post- & pre-bond
  • Practically no (or little) industry-affordable pre-bond test method
  • Relying on post-bond test only could be costly
  • Must close gap b/w TSV technology and TSV defect

Understanding of TSV from technology development standpoint: Process

<table>
<thead>
<tr>
<th>Is this defect hazardous?</th>
</tr>
</thead>
<tbody>
<tr>
<td>To what degree of defect can the function tolerate?</td>
</tr>
</tbody>
</table>

Understanding of TSV from DFT/test standpoint: Defect
• Memory + SOC first
• Scalable and reconfigurable/flexible TAM even in Mem + SOC
• Let’s try to do what we can now: Post-bond
  • Direct access test for memory chip in post-bond?
  • BIST in SOC to test Memory?
  • TSV interconnect test
    - Stuck-at fault model
    - Delay fault model
    - Crosstalk fault model
• Redundancy and repair
  • A matter of Benefit-Cost analysis
  • Not too far away, as the number of TSVs increases
• Debug is very important
  • For early yield ramp-up
  • To determine who the culprit is
    - May be incorporating KGDs from many manufacturers
What to Test in Post-bond?

- Issue: Test cost reduction and test quality

Diagram showing pre-bond and post-bond testing with various tests such as Interconnect test, SOC test, Memory test, and Others.
Future perspectives
Future Perspectives

• KGD
  • Reliability testing
  • How good is the KGD?

• What Standard?
  • Two major EDA companies of DFT are driving two different standards
    - IEEE1500/IEEE P1838 v.s. IEEE P1687

• Will LBIST be tempting??

• On-chip instruments? Power? Temperature? ..... 
  • On-chip instrumentation:
    - Voltage droop detector, process monitors, temperature sensors, aging sensors, performance monitors

• DFD
  • Debug utilizing on-chip instruments?
  • Partition system into independently debuggable block
Thank you